Cu-Sn intermetallic bonding for 3D MEMS integration

by

He Liu

Thesis submitted for the degree of

Philosophiae Doctor

Department of Physics

University of Oslo

January, 2014

Series of dissertations submitted to the
Faculty of Mathematics and Natural Sciences, University of Oslo
No. 1490

ISSN 1501-7710

Cover: Inger Sandved Anfinsen.
Printed in Norway: AIT Oslo AS.

Produced in co-operation with Akademika Publishing.
The thesis is produced by Akademika Publishing merely in connection with the thesis defence. Kindly direct all inquiries regarding the thesis to the copyright holder or the unit which grants the doctorate.

Abstract

3D integration is an emerging technique which features vertical stacking of chips to achieve high performance, low cost and multifunctional packages. In the heart of 3D integration development is the interconnection technique used between dies. The objective of this work is to utilize Cu/Sn intermetallic bonding to develop reliable, low cost and robust interconnect techniques for 3D die stacking, with major focus on heterogeneous stacking scenarios.

This thesis has introduced a novel fluxless Cu-Sn SLID bonding approach, where an intermetallic Cu_3Sn layer is applied as the oxidation barrier for Cu interconnects.Oxidation behavior of intermetallic Cu_3Sn was investigated by aging Cu and Cu/Cu_3Sn multilayer-films at elevated temperatures in ambient air, and by measuring the oxidation level with energy dispersive x-ray spectroscopy (EDX).

Cu/Sn to Cu/Sn dual layer SLID bonding of interconnects was carried out at wafer level. A major advantage of the Cu/Sn to Cu/Sn bonding scenario is avoiding the dynamic wetting of molten Sn to Cu, and replacing with a liquid to liquid integration. The bonded interconnects showed shear strength of 45 MPa and electrical resistance on the order of 100 mΩ.

Processing challenges of Cu-Sn SLID bonding were addressed in this thesis. Sn overflow problem in a Cu-Sn SLID system was solved by designing a margin of 15 μm at the Cu pads to tolerate Sn spreading; Approaches to meet uniformity requirement for electroplated Cu and Sn layers, which is crucial for achieving successful wafer-level bonding without a chemical mechanical polishing (CMP), has been proposed. Uniformly deposited Cu layer with 4% height variation across the wafer, has been achieved by combining pulsed-reversed plating and optimization of electroplating mask.

Comprehensive study of material properties and the influence of process parameters have been carried out. The mechanism of interdiffusion and reaction between the metals used during wafer-level SLID bonding has been investigated by studying the microstructure evolution of the intermetallic compounds Cu_3Sn and $Cu_6Sn_5$for samples exposed to temperatures up to 400 ^oC; The bonding time, required to achieve a single intermetallic compound (IMC) phase (Cu_3Sn) in the interconnects, was estimated based

on the parabolic growth law with consideration of defect-induced deviation; Correlation between the grain size and the interdiffusion rate has been analyzed based on data acquired in this study and in literature, where various deposition methods lead to different grain size; The influence of temperature ramp rate at the beginning of the bonding process has been studies by annealing Cu/Sn film with various temperature ramp rate. Low temperature ramp rate can potentially improve the integrity of the interconnects by reducing voiding and the risk for fracture.

Acronyms

3D	Three dimensional		**PoP**	Package on package
ASIC	Application-specific integrated circuit		**PR**	Photoresist
BAR	Bulk Acoustic Resonator		**RF**	Radio frequency
BGA	Ball grid array		**RT**	Room temperature
CMOS	Complementary metal–oxide–semiconductor		**SEM**	Scanning electron microscopy
CMP	Chemical-mechanical polishing		**SIP**	System in a package
CPU	Central processing unit		**SLID**	Solid-liquid interdiffusion
C2C	Chip to chip		**SoC**	System on a chip
C2W	Chip to wafer		**STD**	Standard deviation
EDX	Energy dispersive X-ray spectroscopy		**TLP**	Transient Liquid Phase
FEM	Finite element method		**TPMS**	Tire Pressure Measuring System
FIB	Focused ion beam		**TSV**	Through silicon via
IC	Integrated circuit		**TX**	Transceiver
IMC	Intermetallic compound		**W2W**	Wafer to wafer

KGD	Known good die		**WLP**	Wafer Level Packaging
MCM	Multi-chip module		**µC**	Microcontroller
MEMS	Micro-electrical-mechanical Systems			
PCB	Printed circuit board			

Preface

This thesis is submitted in fulfillment of the requirements for the degree of Philosophiae Doctor at the University of Oslo, Norway.

The work presented in this thesis was performed at the Department of Micro and Nano Systems Technology (IMST) at Vestfold University College in Horten. The project is funded by the Research Council of Norway (NFR) under project No. 174320, "3DHMNS - 3D Heterogeneous Micro-Nano Systems". Investigation with focused ion beam was carried out at University of Colorado, Boulder, with assistance from Joseph Brown.

I want to express my sincere gratitude to my advisors Nils Høivik and Knut E.Aasmundtveit. Without their support and understanding I would have never gone this far.

I would like to thank all the members, current and former, of our 3D packaging research group, for their collaboration, companionship, and advices.

I would like to thank our research partners at SensoNor AS during the project: Terje Skog, Gjermund Kittilsland and Birger Stark, for their collaboration, support, and insight.

I thank Einar Halvorsen and Xuyuan Chen for their guidance both professionally and personally.

I would like to thank my husband Guangmin Ouyang, my mother Yingjie Zhu, and my farther Jingshan Liu, for their constant support all through the years.

January, 2014

He Liu

List of articles

I. **H. Liu,** E. M. Husa, Z. Ramic, A. Munding, K. Aasmundtveit and N. Hoivik, “Uniformity requirements for electroplated Cu-Sn interconnects used in heterogeneous 3-D MEMS/ASIC stacks", in Proceedings of IMAPS Nordic, September 14-16, 2008, Helsingør, Denmark.

II. **Liu, H.**, Wang, K., Aasmundtveit, K., Hoivik, N. , "Intermetallic Cu_3Sn as oxidation barrier for fluxless Cu-Sn bonding", Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th , pp.853-857, 1-4 June 2010.

III. Hoivik, N., **Liu, H.**, Wang, K., Salomonsen, G, Aasmundtveit, K.E., "High-temperature Stable Au-Sn and Cu-Sn interconnects for 3D stacked applications," Advanced materials and technologies for micro/nano-devices, sensors and actuators: proceedings of the NATO advanced research workshop on advanced materials and technologies for micro/nano-devices, sensors and actuators 2010.

IV. **Liu, H.**, Salomonsen, G., Wang,K., Aasmundtveit, K.E. Hoivik, N. "Wafer-level Cu/Sn to Cu/Sn SLID-bonded Interconnect with Increased Strength", IEEE transactions on Advanced Packaging. 2011; 1 (9): 1350-1358.

V. **Liu, H.**, Wang, K., Aasmundtveit, K., Hoivik, N. "Intermetallic Compound Formation Mechanisms for Cu-Sn Solid-liquid Interdiffusion Bonding", Journal of Electronic Materials, vol. 41, pp. 2453-2462, 2012.

Contents

1 Introduction

1.1 3D heterogeneous integration

3D integration and packaging has drawn more and more attention during the past few years. Worldwide academic and industrial research is focused on technology innovation, evaluation and realization. 3D integration is an emerging, system level integration architecture wherein multiple strata (layers) of planar devices are stacked and interconnected using through silicon (or other semiconductor material) vias (TSV)[1].2D scaling has been driving the size shrinking, cost reduction and performance optimization of electronics for the past few decades, as predicted by Gordon E. Moore back in 1960-1970s (Moore's law has predicted that the number of transistors that is placed inexpensively on an integrated circuit doubles approximately every two years[2].).The major contributor to achieve this is the continuous increasing capability of photo lithography technology. However, Moore's law will hit its fundamental limit in the near future.16 nm lithography pitch will result in 5 nm gate length, at which tunneling effects start to occur[3]. Not to mention the extreme high costs associated with equipment to achieve such fine lithography. Vertical integration is the one of the most promising technology approaches to further develop more sophisticated silicon based electronic components and systems.

Heterogeneous integration is one of the most important reasons to consider 3Dintegration. As Moore's law reaches the physical limit, the integration of non-digital functionality into a package would provide more value to the semiconductor industry. This approach is sometimes addressed as the "More than Moore" concept. The compactness of a certain system is less relying on the scaling of the IC, but on the integration of various functionalities into a compact device. Fig. 1 shows a vision of a future highly integrated system with many different modules, such as digital, analog, biotech, optotech, MEMS, RF, and even power modules.

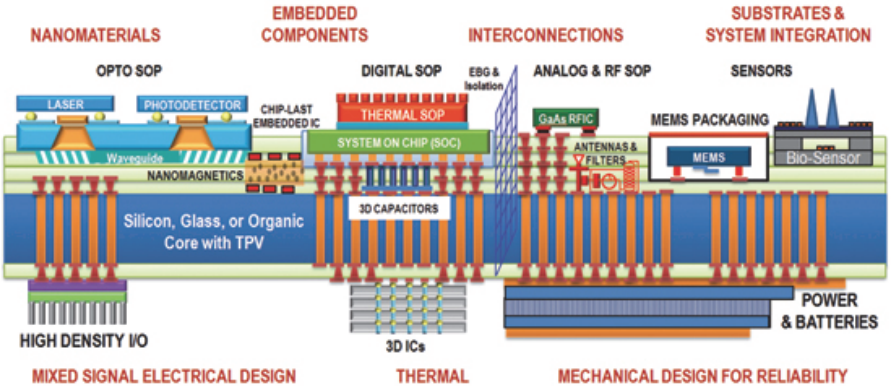


Fig. 1 A vision of future 3D hyper-integration of infotech, biotech, optotech, MEMS and power modules-a new paradigm for future technologies. (Source: GeorgiaTech[4])

One way to achieve multifunctional electronic systems in a 2Dmanner is the so called “system on a chip” (SoC), which may contain digital, analog, antenna, power management and even mechanical sensors on a single chip. However, the realization of true SoC devices with a large variety of functional blocks is very difficult to achieve. Technologies need specific optimization for logic, analog, memory, etc., to reach the desired performance levels and circuit density. To achieve a high cumulative yield, which is determined by multiplying the yield of each module of the hybrid circuit, can be challenging. It becomes even more difficult to integrate MEMS and IC in a single chip economically. MEMS-CMOS monolithic integration is limited to certain applications. Pre-CMOS micromachining require the wafer to meet stringent criteria, e.g., with respect to contaminations, to be able to enter a microelectronic processing line afterward; Post-CMOS micromachining is limited to a stringent thermal budget to about 400^{o}C, or the CMOS interconnect metallization has to be modified to high temperature tolerance for the add-on fabrication steps[5]. For non-silicon MEMS technologies which utilize polymer, glass, or ceramics as substrate, monolithic integration becomes challenging, and in some cases impossible. A traditional hybrid integration approach is to fabricate MEMS structures and ASICs using different processes optimized for each of the technologies, and combine both chips in a leadframe/package, as shown by the few examples in Fig. 2. A large form factor for this system is inevitable using this approach, and the interconnection by wire bonding may lead to signal integrity issues and more power

consumption in some applications. 3D integration, as shown in Fig. 2, enables compact devices and better electrical performance.

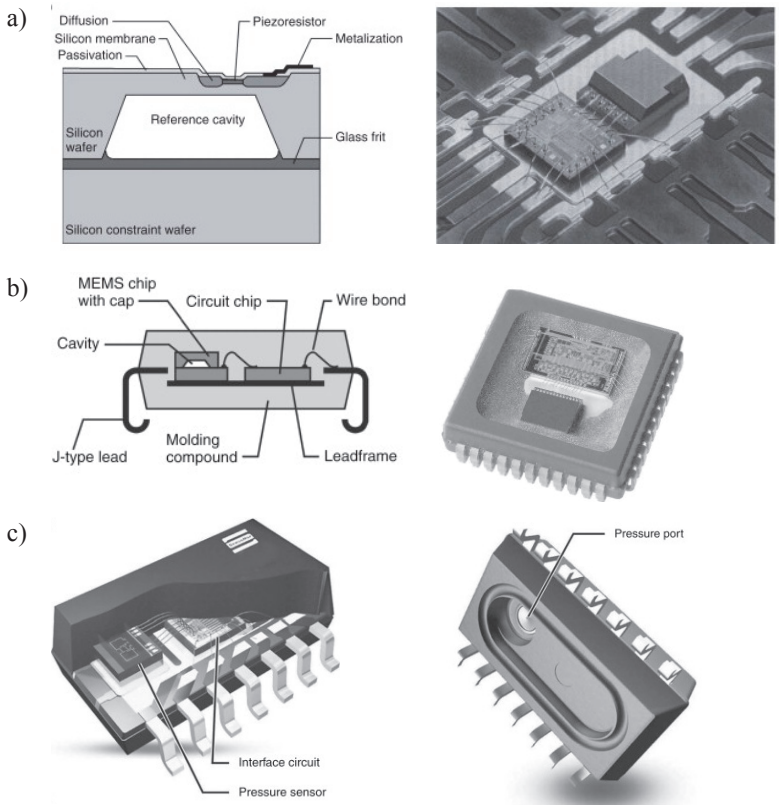


Fig. 2 Examples of traditional 2D integration of MEMS and ASIC on a lead frame.a) Left: Schematic of piezoresistive pressure sensor by Freescale Semiconductor (formerly Motorola) bonded to silicon constraint wafer using glass frit bonding. Right: Photograph of Freescale acceleration sensor and interface circuitry chip mounted on common leadframe; the surface-micromachined accelerometer is protected by glass-frit-bonded wafer cap. (Photo courtesy: Freescale Semiconductor, Austin, TX, USA.) b) Left: Schematic cross-section through postmolded plastic package with J-type leads; the package houses a capped MEMS chip and a circuitry chip on a common leadframe; Right: Photograph of angular rate sensor by Robert Bosch GmbH packaged in postmolded plastic package (44-pin Plastic Leaded Chip Carrier); the molding compound on top of the package is partly removed to show the location of the wafer-bonded sensor chip and the interface circuit. (Photo courtesy: Robert Bosch GmbH, Reutlingen, Germany.) c) Left: Schematic of packaging concept with triplestack sensor chip and interface circuitry, die and wire bonded to leadframe; Right: Schematic of postmolded pressure sensor

package with pressure access port. (Images courtesy: Infineon Technologies SensoNor AS, Horten, Norway.)[6]

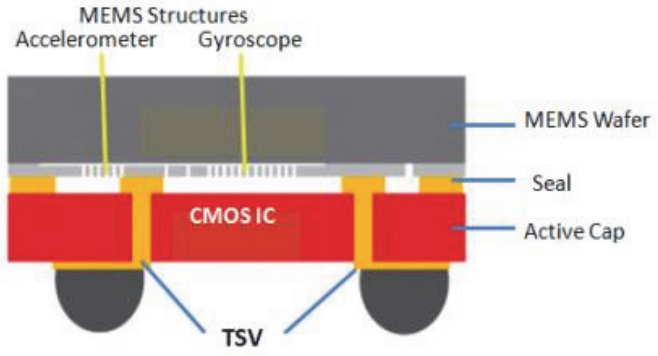


Fig. 3 Schematic drawing of MEMS inertial sensor vertically integrated with CMOS IC by STMicroelectronics[7]. Using TSV through the CMOS IC chip enables active capping and eliminates the use of the bond wires at the same time.

A primary application for 3D integration is portable devices such as mobile phones, laptop computers, tablets and personal digital assistants (PDA). What these devices have in common is the small size, which again requires smaller and smarter integration of the electronic components. Automotive is also a promising field since light weight, small form factor sensors are desired. Personal medical devices to monitor abnormal human functionality, such as brain or heart diseases are also an interesting field since compactness and light weight is most desired in such applications. As a result of both technology push and consumer demands, future applications will require communication, sensing and power modules to be integrated together with the processing unit and memory, to achieve a smart system in a single package.

1.1.1 Evolution

Back in1998, U.C Berkeley initiated the “Smart Dust” project, which aimed to pack an autonomous sensing, computing, and communication system into a cubic-millimeter mote (a small particle or speck) to form the basis of integrated, massively distributed sensor networks[8, 9]. The project was completed in 2001, although Pister and his group

did not achieve the dust–size (one cubic millimeter) system as they have first targeted[10].However, the idea of autonomous device and vertical integration of electronic components has inspired the technology community to bring the concept forward. Similar activity was initiated in Europe in 2006[11]. The integrated EU project e-CUBES goal was to advance microsystem technologies for cost effective realization of highly miniaturized, truly autonomous systems for ambient intelligence[12-15]. Also initiated in 2006, The DAVID(downscaled assembly of vertically interconnected devices) project targeted to provide an extremely high packaging density for hybrid integration of MEMS with ASICs[16]. 3D integration has made tremendous progress during the past decade. Wafer thinning, through silicon via (TSV) technology, metal-to-metal bonding, thermal models were all developed and used within the e-CUBES project. These optimized 3D integration technologies were successfully implemented for Infineon's automotive demonstrator, a tire pressure measurement system (TPMS), as shown in Fig. 4, to validate technological solutions for the fabrication of high value-added heterogeneous components and systems. The DAVID project has demonstrated W2W integrated MEMS inertial sensor with ASIC capping, as shown in Fig. 5.

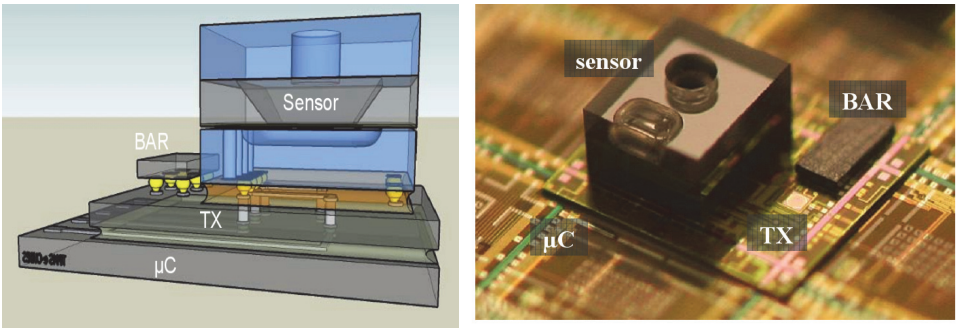


Fig. 4 3D integrated MEMS/IC systems for Infineon´s TPMS wireless sensor nodes (e-CUBES). This demonstrator consisted of a microcontroller (µC), an RF transceiver (TX), a bulk acoustic resonator (BAR) and a pressure sensor from SensoNor AS.[1]

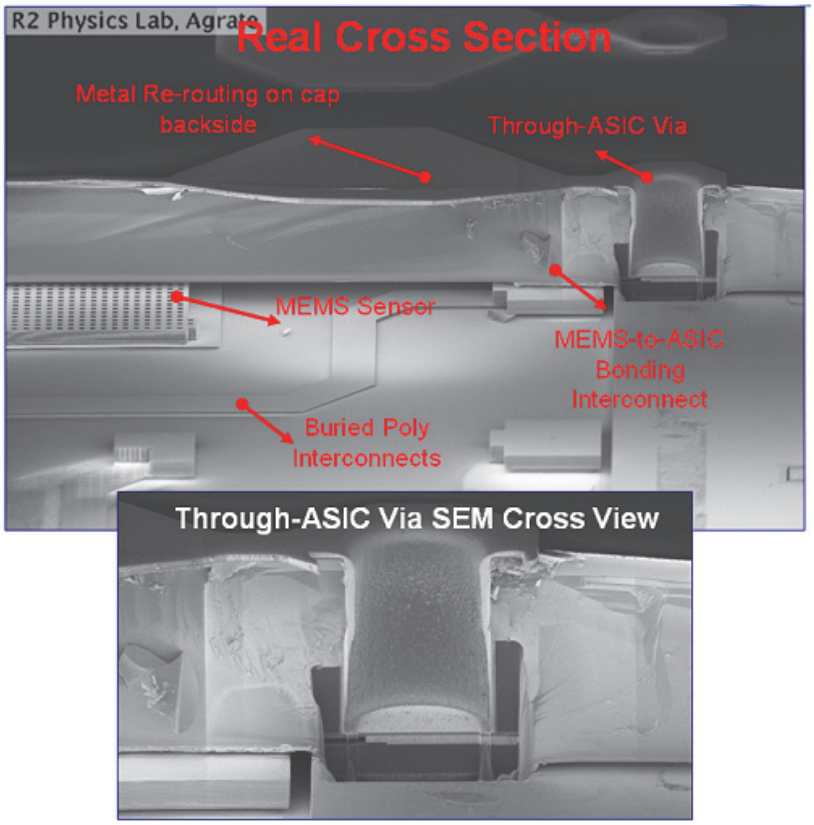


Fig. 5 Cross-section view of the DAVID wafer-to-wafer (W2W) bonded demonstrator. (Source: Fraunhofer). MEMS hermetic sealing and vertical interconnection between the MEMS sensor and the ASIC cap was achieved in a single fabrication step using Au-Au metallic bonding. [2]

Building on the success of e-CUBES, the e-BRAINS project was initiated September 2010[17]. The target of the project is to develop 3D heterogeneous integrated systems with improved reliability, robustness and reproducibility. This project has three-year time-frameand is still on-going to this date.

As of today, there are commercial products where the MEMS is stacked with ASIC available, although not yet with integrated RF module, batteries etc. Examples are gyroscopes and accelerometers from InvenSense and Murata (former VTI technologies)[18, 19]. A cross section view of VTI's 3d integrated MEMS sensor is shown in Fig. 6. VTI has addressed this approach as Chip-on-MEMS, which is based on a

combination of wafer-level encapsulation, wafer level packaging (WLP) technology and chip-to-wafer bonding technology.

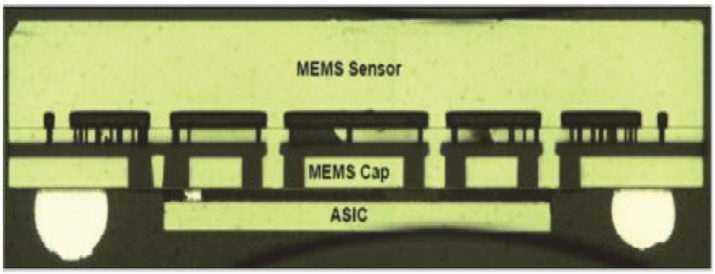


Fig. 6 VTI's 3D integrated MEMS sensor by chip-to-MEMS approach.

The global roadmap in Fig. 7 by Yole development in 2012 has shown the advances of 3D integration in various fields of application. It is seen that 3D integration of MEMS with ASIC capped by TSV is expected to become commercially available by 2016. The ultimate heterogeneous integration of various elements, such as RF module, digital IC, analogue IC, memories and MEMS, is not expected in production until 2018.One essential factor for multi-chip integration is a bonding technology, which enables multiple die stacking, without re-melting previous bonded interconnects. A promising technology is Cu-Sn solid-liquid-interdiffusion bonding, which will be introduced in Section 1.2.

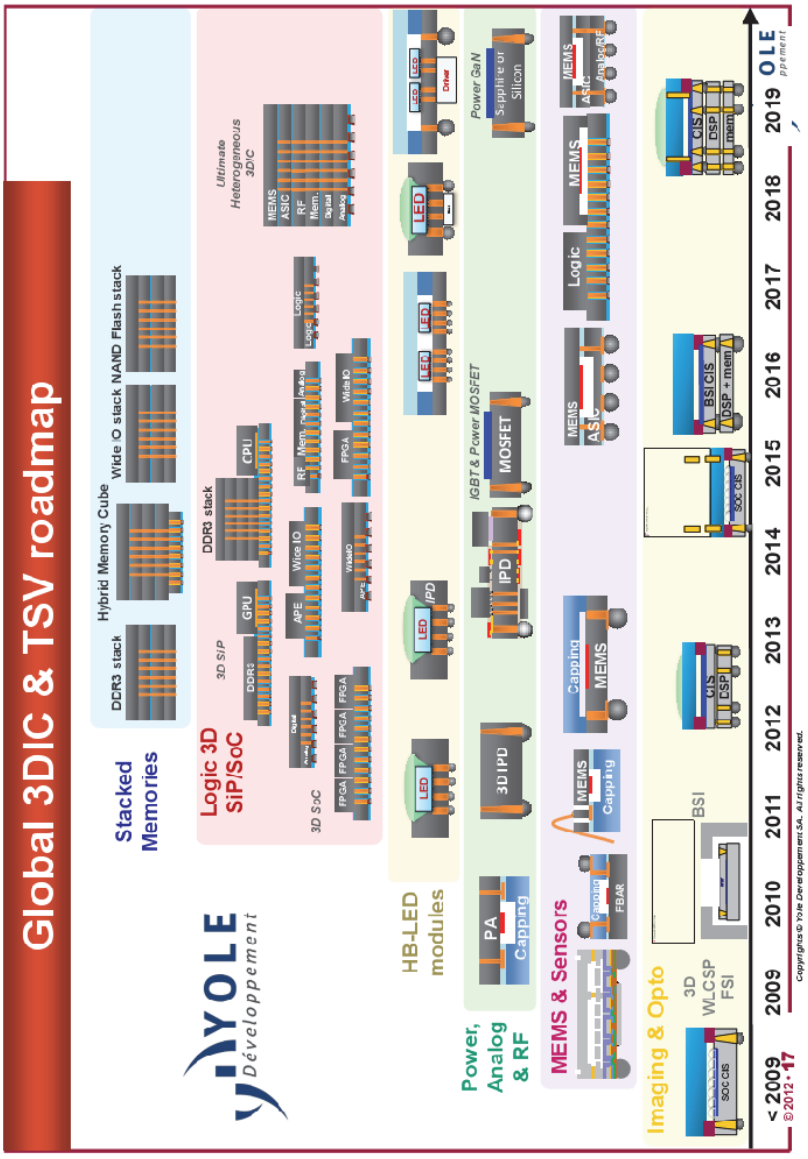


Fig. 7 Global roadmap for 3D integration by Yole development, 2012 (Source: Yole development) [20, 21]

1.1.2 Integration schemes and enabling technologies

Enabling technologies for 3D integration includes: (i) Thinning of the strata (ii) through-silicon (or other semiconductor materials) vias (TSV); (iii) bonding between stacked dies; (iv) power delivery and cooling solutions. A schematic drawing of such stacked dies is shown in Fig. 8. This thesis focuses on developing interconnection between dies by metal bonding. Such interconnections can be achieved either simultaneously or sequentially. The simultaneously reflow approach requires the dies to be placed by a precision placement tool, and held in place with a tacky flux before the reflow process. The simultaneous joining of multiple chips can be achieved within a single reflow step. However the approach raises very high requirement for the placement process to allow the self-centering effect for the solder bumps to accommodate the potential displacement between chips[22].For sequential stacking, one of the major challenges associated with stacking multiple dies is to ensure that subsequent bonding will not re-melt and damage the interconnections between previously bonded entities. Sn-alloy soldering, as the most commonly used interconnection technique in the semiconductor industries, is not practical for such applications, due to the need to use different solder composites for each level of interconnection, to ensure reasonable differentiation in melting temperature, not to mention that the bonded interconnects have to withstand subsequent level 1 and level 2 packaging[23]. (Bonding a die to a substrate and further encapsulation is denoted as level 1 packaging; Mounting of the encapsulated die to a printed circuit board (PCB) is denoted as level 2 packaging.) In traditional flip-chip technology, this has been accomplished using high-temperature Pb-rich solder for chip-to-substrate bonding, and standard solder for the next level of packaging. Note that using Pb-rich solder is not an environmentally friendly solution, and is currently being replaced with Pd-free alternatives. One of these alternatives is Au-Sn solder, but the challenge for any sequential solder process is the limited number of different solder temperatures that are practically available. For a process requiring more than 2-3 sequential solder steps, it is hardly realistic to set up a process temperature budget with sufficient margin for all solder steps. Therefore, an excellent approach to resolve this issue is to use solid-liquid interdiffusion bonding, which has the capability to withstand the same processing temperature repeatedly once the joint is formed. This technique will be introduced in Section 1.2.

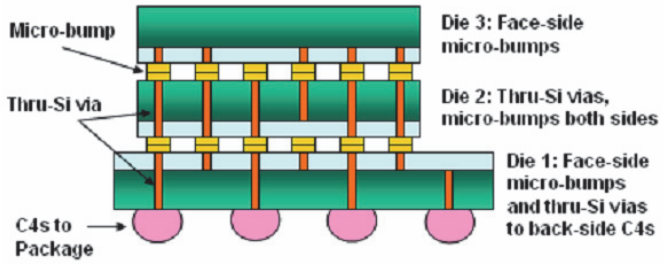


Fig. 8 Schematic illustration of 3D integration achieved by wafer thinning, TSV and wafer bonding [24].

To achieve interconnection between dies, various bonding schemes can be applied, including chip to chip (C2C), chip to wafer(C2W), and wafer to wafer(W2W) bonding.

W2W method has the highest throughput and is potentially the most economical way of integration. However the method has its limitations. First of all, for MEMS applications, it is very common that the MEMS die and ASIC are produced on different wafer sizes, thus not being compatible with a W2W approach. Even if the wafer size is identical, the MEMS and the ASIC will typically have different chip areas. In such cases, W2W integration therefore results in waste of wafer area. Secondly, the bonded module may suffer from reduced overall yield, because good dies may be bonded with bad ones. When combining n untested dies from wafers with a die yield Y_i, the compound yield of the structure Y_m will be:

$$Y_m = Y_p \cdot Y_i^n \qquad (1)$$

Where Y_p is the yield of the interconnect and packaging process.

With low manufacturing yield for individual wafers, multiple stacking results in exponentially smaller module yields, e.g., if $Y_p = Y_i = 95\%$, number of tiers to integrate n=4, the module yield Y_m is only77%. Such yield loss is inevitable when using W2W bonding techniques. Therefore, W2W bonding scenario raises high requirement of ensuring high yield on individual wafers.

The C2C method is flexible and not limited by different die size, wafer size or yield on individual wafer. One can mix-and-match preferred technology into a smart assembly. Dies can be tested before C2C integration to ensure higher yield for final assembly. This approach is addressed as known good die (KGD) method. An obvious drawback for C2C bonding is the overall throughput compared with wafer-level integration.

The C2Wmethod gives moderate throughput, but it is much more flexible than W2W bonding. Die sizes can be different between tiers, and the KGD method can be used to boost the overall yield.

C2C and W2W bonding processes are both investigated in this work, while C2W bonding is out of the scope of this thesis.

1.1.3 Bonding technologies for 3D MEMS integration

Bonding, which provides mechanical and electrical interconnection between stacked dies or wafers, is a key step for 3D integration. Table 1 has summarized the metal bonding techniques that can be used for interconnection for 3D MEMS integration. The choice of bonding techniques can depend on:

1. Requirement from the application.
    - Connection density between stacked dies.
    - In-field environment of the final product.
2. Whether the bonding technique can fit into the process flow.
    - The temperature budget.
    - Added material that might cause contamination to post-processing line.
    - Flux or other organic contamination introduced by the bonding process to sealed cavities.
3. Cost and throughput.

This thesis is focused on Cn-Sn SLID bonding, which will be introduced in the next section.

Table 1 Comparison of bonding technologies that can be used for 3D Microsystems integration

	Temperature (^{o}C)	**Bond strength (MPa)**	**Bonding time (min)**	**Advantages**	**Disadvantages**
Au-Sn Eutectic bonding	278	26-90 [25]	2-30 [25]	High stability against oxidation.	Au contamination. Difficult for stacking of multiple dies.
Solder bonding	200-300			Well understood.	Difficult for stacking of multiple dies. All deposited pattern must be of the same size and shape.
Cu direct bonding	RT bonding 200-400 annealing[4]		30-120 min annealing [4]	No added material.	High requirement to surface roughness. In situ cleaning needed.
Cu-Cu thermal compression bonding	400@4000mBar[26]	50[27]	30 [26]	No added material.	In situ cleaning needed.
Metal/adhesive (or metal/oxide) hybrid bonding	Material dependant.			Interconnection and underfill achieved in one step.	Compatibility of materials need to be qualified.
Cu-Sn SLID bonding	260-300	11-114 [28-31]	20-30	Suitable for multiple die stacking.	Not reworkable. Cu is prone to oxidation.

1.2 Solid-liquid interdiffusion bonding

SLID technology is based on the rapid formation of intermetallic compounds between a high-melting point component (in this case, Cu) and a low melting point component (in this case, Sn) at a temperature above the melting point of the latter. A phase diagram of the binary system is shown in Fig. 9. When the temperature is raised to the melting point of Sn, Cu diffuses into liquid Sn rapidly and intermetallic compounds (IMCs) grow much faster than solid state diffusion and IMC formation below the Sn melting point. At the processing temperature (260°C -300°C), two intermetallic phases, Cu_3Sn (ε-phase) and Cu_6Sn_5 (η-phase), exist. The melting points of these two IMCs are 676°C and 415°C, respectively, and the metal joint therefore solidifies once the IMCs are formed. This unique process is also referred to as iso-thermal solidification, off-eutectic bonding or transient liquid phase (TLP) bonding in the literature [32-35]. Cu-Sn SLID bonding was first introduced to the semiconductor applications by Bernstein in 1966[36]. With the rise of 3D integration, Huebner identified SLID bonding as a suitable approach for die stacking in back in 2002, where he successfully demonstrated SLID bonding of thinned silicon dies[30]. During Cu-Sn SLID bonding, Cu_6Sn_5 is the first phase to be formed upon solidification. As the interdiffusion continues, Cu_3Sn is formed continuously by consuming the Cu_6Sn_5 and Cu. Finally, Cu_3Sn becomes the only IMC phase present as long as there is surplus of Cu in the binary system [37]. The final bonded interconnect, comprising of Cu and Cu_3Sn, reaches a thermo dynamic equilibrium and long-term stability. The melting point of formed IMC is well above the processing temperature and the bonded interconnect can therefore tolerate the same temperature repeatedly to stack more dies if needed. Using electroplating to pattern and deposition Cu and Sn the interconnects can be fabricated at relatively low cost [30, 31, 37, 38]. Furthermore, it has been demonstrated that this interconnection technique can be used to create hermetic sealing and encapsulation for MEMS devices [31, 39-41]. Development of Cu-Sn encapsulation is an on-going work in our group at IMST[42, 43].

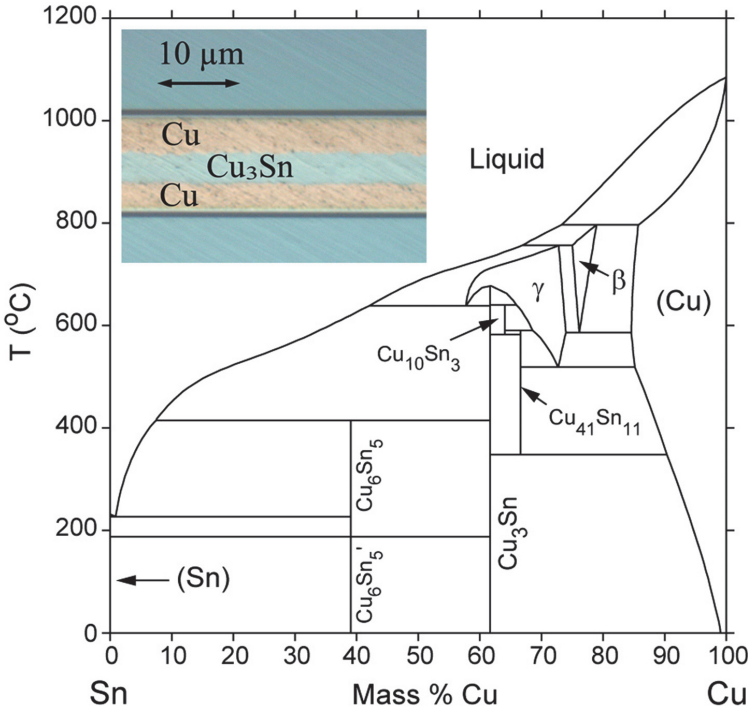


Fig. 9 Cu-Sn phase diagram[44]. The inset shows a cross-section of Cu-Sn SLID bonded interconnect, where the middle IMC layer is a single phase: Cu_3Sn.

1.2.1 Fabrication and processing methods

A schematic drawing for the test devices is shown in Fig. 10. In this work, silicon substrates were used for most of the test devices. A silicon dioxide layer is required between the metal and Si for electrical isolation. On top of the oxide layer, NiCr or TiW alloys are employed as a diffusion barrier layer to retard Cu diffusing to the Si substrate. They also act as the adhesion layer between the substrate and the electroplating seed layer (Au or Cu). Electroplating of Cu and Sn is chosen as the deposition method, due to the large deposition rate and low cost. Alternative deposition methods are sputtering and evaporation, which give improved purity, but are very slow and expensive. Moreover, these processes are more likely to introduce stress in the deposited metal due to the high temperature used during deposition. Therefore electroplating is the most commonly used deposition method for thicker films and for Cu-Sn SLID bonding [33, 34, 37, 45]. Through-mask electroplating is employed to define the bump pattern for electroplating.

One challenge with electrochemical deposition is the uniformity of the deposited pattern, especially for applications where interconnect bump and seal frame are deposited in the same step, as will be discussed in Article I and IV.

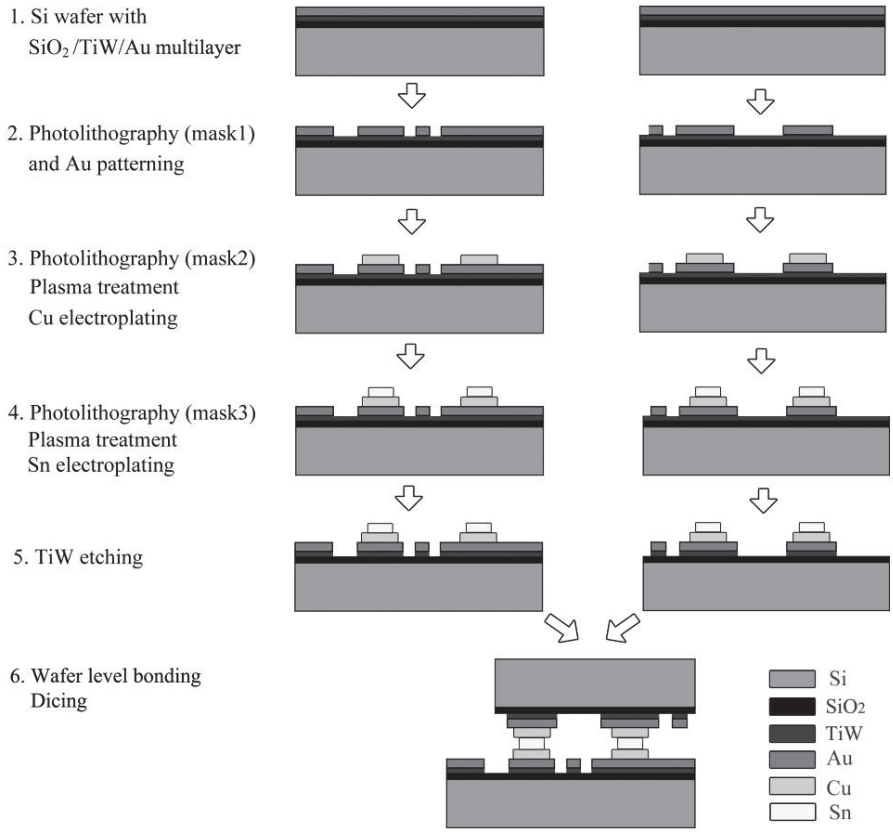


Fig. 10 Illustration of process flow for Cu-Sn SLID bonding.

In Cu-Sn SLID bonding, it is required that there is surplus of Cu with respect to Cu_3Sn formation. This is to ensure that Cu_6Sn_5 is fully converted to Cu_3Sn so the metal system reaches a thermal equilibrium and becomes stable. The calculation of the minimum required thickness ratio from the composition of the intermetallic compound Cu_xSn_ycan be performed as follows:

$$\frac{h_{Cu}}{h_{Sn}} = \frac{V_{cu}}{V_{Sn}} = \frac{x}{y}\frac{M_{Cu}\rho_{Sn}}{M_{Sn}\rho_{Cu}} = 1.31$$

where h_{Cu} and h_{Sn} denote the layer thicknesses of Cu and Sn, V the respective volumes, M their molar masses, and ρ their density. Material properties of Cu and Sn are given inTable 2. In this work, 10 μm of Cu and 3-4 μm of Sn are used for SLID bonding.

Table 2 Material properties for Cu, Sn and their IMC phases present in Cu-Sn SLID bonding [46].

Properties/ Material	M [g/mol]	P [g/cm^3]	M/ ρ [cm^3/ *mol*]	Melting temperature [^{o}C]
Cu	63.55	8.92	7.12	1084
Sn	118.71	7.28	16.31	232
Cu_3Sn-ε	309.35	8.9	34.76	676
Cu_6Sn_5-η	974.83	8.27	117.86	415

After electroplating and removal of the photoresist, the wafers are cleaned by acid (e.g.5% HCl) and Ar+ O_2plasma prior to bonding. Both wafer level and chip level bonding were studied in this thesis. In order to investigate the integrity of the boned interconnect, die shear testing, cross-section polishing and metallurgy inspection was performed. Focused ion beam(FIB), scanning electronic microscopy(SEM), and energy dispersive x-ray spectroscopy (EDX) are used for material morphology examination. A four-probe resistance measurement structure is designed by utilizing electroplating seed layers as conductive traces and probing pads. Details of the resistance testing method are reported in Article IV.

1.2.2 Technology focus of this thesis

Electrochemical deposition

One challenge in electroplating is the uniformity of the deposited metal. Typically, the non-uniformity across a wafer is between 5 to 10%. It is in the nature of electro-deposition that the growth rate of metal depends on the local charge flux density, which further depends on the electric field distribution in the electrolyte. The electric field in the electrolyte depends on the geometry of the electrodes (both cathode and anode), and

the geometry of the electrolyte (as a liquid, the geometry of the electrolyte is determined by the container that holds it). Chemical-mechanical polishing (CMP) after electroplating is therefore often used to reduce any height variation across the wafer. However, it can be challenging to implement CMP for wafers with fragile MEMS structures due to stress and chemicals introduced by the CMP process. Post-CMP cleaning for MEMS structures with cavities can be difficult because slurry particles can get trapped.

For wafer-level bonding, the uniformity of the electroplating across the wafer is important for successful bonding, and high bonding yield. During bonding using Cu-Sn, the Sn layer will be compressed and melted, and can tolerate some height variation (similar to the solder collapse in a solder reflow process); while the Cu layer remains in solid phase. Hence any grave non-uniformity across the Cu features will affect the bonding integrity. Generally, the total height variation (Maximum-Minimum) from Cu pads at both sides of the wafer and between interconnects should not exceed the thickness of the Sn. Contacts can still be made by providing sufficient bonding pressure. Moreover, the average height of each pad should be uniform, to avoid squeezing out excessive Sn.

With optimization, Cu electroplating with 4% non-uniformity across wafer was achieved with a general purpose electroplating tools in IMST lab. Detailed approaches are referred to Article I, III and IV.

Single Cu_3Sn phase – thermal equilibrium

It is preferable that the final bonded joint consists of a single Cu_3Sn phase sandwiched between Cu, rather than a bond line with a mixture of Cu_6Sn_5 and Cu_3Sn, since the Cu_6Sn_5 will continue to transform to Cu_3Sn (Cu_3Sn formation is observed at a temperature as low as 60^oC[47].) and with it the mechanical properties of the interconnect will change. It has been reported that during the formation of Cu_6Sn_5,tensile stress is developed in the film, and when the Cu_6Sn_5 is converted to Cu_3Sn, a compressive stress is developed [48]. For SnAgCu solders, the interfacial diffusion and reaction between Cu and Snare the major reasons that fractures initiate after aging and thermal cycling, and thus compromise the reliability of the solder joints [7]. One advantage of Cu-Sn SLID bonding to Sn-based soldering, is that all the Sn in Cu-Sn binary system will be transformed to Cu_3Sn, thus the bond line reaches a thermal equilibrium. The mechanical-electrical properties will not change after the bond is made. Unlike Cu_6Sn_5, which grows rapidly during solid-liquid interdiffusion, Cu_3Sn formation relies on solid phase

interdiffusion between Cu and Cu_6Sn_5 layers. This requires a sufficient bonding time to allow complete transformation. Possible ways to estimate required bonding time for completed transformation to Cu_3Sn are discussed in Article V.

Wetting, morphology, and Sn overflow

IMC structure and morphology play an important role in terms of material properties and reliability. Therefore a clear understanding of the IMCs formation mechanism and the process parameters is essential.

During Cu-Sn SLID bonding, because Cu atoms have high mobility in the molten Sn, the dissolution and diffusion rates are also very high. The formed IMC is instantaneously solidified upon reaction, and becomes a relatively stable diffusing/reacting metal system, while the rest of liquid Sn continues to move and reshape before it can be solidified. The role of surface tension and convection during SLID bonding has been discussed in Article V.

For Cu-Sn interconnection bonding, the temperature ramping rate can therefore influence the quality of the bonding due to liquid involved convection and surface tension, along with the instant interdiffusion and solidification. Patterning the Cu pads can influence the surface tension and convection of Sn when melting, and therefore influence the interdiffusion flux. Details of the discussions are referred to Article V. Sn overflow is a potential risk for short-circuiting the bonded interconnects. Leaving a margin on the electroplated Cu is one solution to this issue. Details are referred to Article IV.

Bonding environment

For conventional Cu-Sn SLID bonding, a flux agent is required since Cu is readily oxidized in air at the processing temperature (250^oC - 300^oC) [37]. Any surface oxidation of Cu will degrade the surface wettability and induce poor bonding conditions, and therefore lead to low bonding yield [37, 49]. An alternative to using flux during bonding is to pre-clean the Cu surface, and carry out bonding in vacuum conditions, which requires more expensive bonding equipment and further complicates time and temperature control (cooling of dies after high temperature bonding in vacuum is possible, but takes too long time to be practical for a useful process). Moreover, vacuum

bonding is traditionally available with wafer bonding equipment, but not feasible for die level bonding applications.

Furthermore, if an active flux is used during bonding, the flux residues have to be removed afterwards using solvents that are environmentally unfriendly. For flip-chip packaging where the gap between the chip and the substrate can be very small, it is very difficult to completely remove flux residues. Thus, the flux residues trapped in the gap can degrade the performance of the device and may also lead to long-term reliability problems. The flux residue may cause delamination between the underfill/substrate surface and lead to reliability issues[50-55].This work was therefore focused on investigating and demonstrating a fluxless bonding solution for Cu-Sn SLID die bonding for MEMS 3D packaging. In Article II, a successful fluxless die bonding approach using Cu_3Sn as oxidation barrier for the Cu pads is introduced.

1.3 Outline of the thesis

This thesis work started in September 2007 when Infineon SensoNor AS proposed a challenge with regards to 3D packaging of their MEMS pressure sensors. The general aim was to identify an efficient interconnection technology that is suitable for heterogeneous MEMS/ASIC die stacking. A further aim is to implement and characterize such interconnect technology to evaluate its feasibility for commercial MEMS devices. A few technical challenges were discovered along the way, such as electroplating uniformity and the influence on successful bonding, ensuring single Cu_3Sn phase for a reasonable bonding time. My goal was therefore extended to find suitable solutions to these challenges and making the developed process feasible for an industrial process. Electroplating uniformity is discussed in Article I and IV, and minimum time to ensure total transformation of Cu_3Sn is discussed in Article V.

Another aim was to optimize the process in terms of throughput, cost and reliability. With these purposes in mind, a wafer-level bonding process of Cu/Sn to Cu/Sn bumps has been demonstrated on dummy wafers, as was presented in Article IV; A fluxless bonding approach on chip level has been investigated using Cu_3Sn as oxidation retardation layer, as was presented in Article II; Efforts were exerted to understand IMC formation, voiding

mechanism, Sn flooding, etc., with the aim to improve reliability of the interconnects (Article V).

2 Summary of articles

2.1 Article I

H. Liu, E. M. Husa, Z. Ramic, A. Munding, K. Aasmundtveit and N. Hoivik, *"Uniformity requirements for electroplated Cu-Sn interconnects used in heterogeneous 3-D MEMS/ASIC stacks",* in Proceedings of IMAPS Nordic, September 14-16, 2008, Helsingør, Denmark.

For non-reflow bonding processes the height uniformity of the interconnects will affect the bond quality and yield significantly. For 3D MEMS/ASIC heterogeneous integration, CMP can be challenging to apply because fragile structure might not be able to tolerate the stress during polishing, and slurries can be trapped in the cavities. For MEMS/ASIC integration, a sealing ring is usually required in conjunction with interconnects, which makes the uniformity of the deposited metal even more critical. It is well known that during electroplating, small features have larger deposition rate than big features. This will bring difficulties to 3D MEMS/ASIC integration, because during electroplating the sealing-ring and interconnects may have different deposition rates due to their pattern difference. In this work, the dependency of the uniformity of the electroplated micro-bumps on the plating geometry is investigated. An optimized electroplating mask was designed, and more uniform bumps were obtained. The optimized mask resulted in an electroplating surface height variation of 13% across the chip, while 33% of variation was observed using a non-optimized mask. Analysis of the electroplated interconnect bumps using the optimized mask are expected to demonstrate sufficient uniformity to achieve bonding.

2.2 Article II

H. Liu, K. Wang, K. Aasmundtveit, N. Hoivik, "Intermetallic Cu_3Sn as oxidation barrier for fluxless Cu-Sn bonding", Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th, pp.853-857, 1-4 June 2010.

A fluxless Cu-Sn SLID bonding process was for the first time demonstrated using intermetallic Cu_3Sn layer as the oxidation barrier for Cu interconnects. Oxidation behavior of intermetallic Cu_3Sn was confirmed by aging Cu and multilayer Cu/Cu_3Sn films at elevated temperatures in ambient air, and measuring the oxidation level by energy dispersive x-ray spectroscopy (EDX). The strength of bonded interconnects were characterized by shear testing, and found to be comparable to conventionally SLID bonded interconnects assembled using flux. Furthermore, the interdiffusion process of elemental Cu and Sn in the bonding region is discussed.

This article was cited at an ECS wafer-level bonding workshop the following year as a noteworthy process worth pursuing for metallic wafer-level bonding. The article is further externally cited seven times as of 2013.

2.3 Article III

N. Hoivik, H. Liu, K. Wang, G. Salomonsen, and K. Aasmundtveit, "High-Temperature Stable Au–Sn and Cu–Sn Interconnects for 3D Stacked Applications," in Advanced Materials and Technologies for Micro/Nano-Devices, Sensors and Actuators, E. Gusev, E. Garfunkel, and A. Dideikin, Eds.,ed: Springer Netherlands, 2010, pp. 179-190.

As second author, my contribution to this publication is the description of the electroplating uniformity modeling, and parts of the experimental work performed for Cu-Sn SLID bonding. The work included in this paper expanded on the initial model developed for interconnects only presented in article I.

It is well known that smaller features (such as interconnects) often become thicker

than larger features (such as seal rings) when electroplated. In order to make the processing compatible for both interconnects and seal-frames, using the same electroplating mask, and achieve interconnection and encapsulation in a single thermal cycle, uniformity across different feature sizes has to be ensured. The pattern density of electroplated interconnects and seal rings require an optimized layout which can be calculated based upon the effective area. Since there is a linear relationship between current density and electroplated thickness, the height of electroplated features can be estimated by simulating the variation of current densities in a mask. Both seal rings and interconnects must be arranged with optimized areas, and pitch, as to minimize any height differences.

2.4 Article IV

H. Liu, G. Salomonsen, K. Wang, K. Aasmundtveit, and N. Hoivik, "Wafer-level Cu/Sn to Cu/Sn SLID-bonded Interconnect with Increased Strength",
IEEE transactions on Advanced Packaging. 2011; 1 (9): 1350-1358.

Flux-less Wafer level Cu-Sn Solid Liquid Interdiffusion (SLID) bonding of interconnects was achieved by bonding two-layered Cu/Sn structures to each other. The bonded interconnects were investigated by mechanical, electrical and microscopic techniques. The Cu-Sn SLID interconnects were created by wafer-level bonding at 260°C. The bonded interconnects show shear strength of 45 MPa and resistance of the order of 100 mΩ. A major advantage of the Cu/Sn to Cu/Sn bonding scenario is to avoid the dynamic wetting of molten Sn to Cu, and simply replace with a liquid to liquid integration. Furthermore, the Sn overflow problem in a Cu-Sn SLID system was successfully addressed by including a margin of 15 μm at the Cu pads to tolerate any Sn spreading. The uniformity requirement for electroplated Cu/Sn layers, which is crucial to achieve successful wafer-level bonding, is discussed. This wafer-level Cu-Sn SLID bonding process is a promising technique for 3-D assembly and packaging. The article is further externally cited four times as of 2013.

2.5 Article V

H. Liu, K. Wang, K. E. Aasmundtveit, and N. Hoivik, "Intermetallic Compound Formation Mechanisms for Cu-Sn Solid–Liquid Interdiffusion Bonding," Journal of Electronic Materials, vol. 41, pp. 2453-2462, 2012.
DOI: 10.1007/s11664-012-2060-3.

The mechanism of Cu-Sn SLID bonding for wafer-level bonding and three dimensional (3-D) packaging applications have been studied by analyzing the microstructure evolution of the intermetallic compounds Cu-Sn at elevated temperatures up to 400 ^{o}C. The bonding time required for achieving a single intermetallic compound (IMC) phase (Cu_3Sn) in the final interconnects was estimated according to the parabolic growth law with consideration of defect-induced deviation. The effect of predominantly Cu metal grain size on the Cu-Sn interdiffusion rate is discussed. The temperature vs. time profile (ramp rate) is critical to control the morphology of scallops in the IMC. A low temperature ramp rate before reaching the bonding temperature is believed to be favorable in a SLID wafer-level bonding process. The article is further externally cited once as of 2013.

3 Summary

3.1 Conclusion

In this thesis, Cu-Sn bonding for 3D MEMS integration applications has been studied. Cu-Sn SLID bonding has been developed and characterized to provide adequate understanding of the processing and material properties, in order to optimize and industrialize this technology.

A fluxless bonding by using Cu_3Sn as oxidation protection layer was successfully demonstrated by C2C bonding. Cu_3Sn IMC has been demonstrated to be more inert to oxidation in air compared to electroplated Cu. By applying this knowledge to Cu-Sn SLID bonding, fluxless bonded dies have been demonstrated with shear strength comparable to conventional Cu-Sn SLID bonding using flux. The average shear strength was measured to 10 MPa. The solid-liquid interdiffusion in the bonding region did not appear to have been retarded by introducing an additional thin Cu_3Sn IMC layer to the Cu layer prior to bonding.

Wafer level SLID bonding was demonstrated with dual-layered Cu/Sn bumps bonded to each other. The measured average shear strength of the bonded interconnects is 45 MPa. The increased shear strength can be due to the advantage of the Cu/Sn to Cu/Sn bonding scheme, where the wetting of molten Sn to Cu is replaced with liquid-to-liquid integration.

The interdiffusion and IMC formation mechanisms during Cu-Sn SLID bonding targeting 3D packaging applications have been discussed. By comparing the interdiffusion coefficient extracted from Cu-Sn systems found in the literature with various deposition methods for Cu, it was concluded that electroplated Cu films with a small grain size is favorable for reducing the overall process time required. For our electroplated Cu-Sn binary system, an activation energy Q for Cu_3Sn is estimated as 100 *kJ/mol*, and the diffusion frequency k_0 is estimated as 2.5 $\times 10^{-10} m^2/s$. A method for simulating the required processing time for Cu-Sn SLID bonding has been proposed by using parabolic diffusion law and Arrhenius equation. Deviation from the parabolic law

has also been discussed and can be included in the calculation to obtain a more reliable and realistic simulation.

Island-shape formation of IMCs with diameters of 300-600 μm has been observed during high temperature rate annealing of Cu/Sn films. A conclusion from this observation is that low temperature rate during the beginning of the bonding potentially improves the integrity of the interconnects by reducing the 'island' size, and therefore reducing the voids at the IMC interface.

The contributions of this research work to the 3D MEMS integration community include:

1. Improved understanding of the processing challenges of Cu-Sn SLID bonding has been provided, targeting 3D integration of MEMS and ASIC. A method to achieve better uniformity of Cu/Sn features fabricated using electroplating, and an approach to reduce Sn overflow during bonding have been introduced.

2. A fluxless bonding method has been developed and demonstrated for Cu-Sn SLID bonding at chip level, using a thin layer of Cu_3Sn to retard oxidation. This approach is promising for MEMS/ASIC integration, since cleaning of flux residue on delicate, sometimes sealed MEMS structure can be avoided.

3. Bonding of Cu/Sn to Cu/Sn dual layered structures has been demonstrated on wafer level with high bond strength. The advantage of this method is that during bonding, liquid-solid wetting is replaced by liquid-liquid merging, and the Cu surface wettability, which is dependent on oxidation and roughness, no longer influences the bond integrity.

The Cu/Sn to Cu/Sn symmetric bonding approach was developed in collaboration with SensoNor technologies AS in the research project, and is the chosen bonding process used for packaging their high-performance uncooled bolometers[40, 41].

4. Improved understanding of IMC formation during Cu-Sn SLID bonding with regards to grain size and temperature ramp rate has been presented. Firstly, processing efficiency is improved by simulations that calculate the time required for fully converting Sn to Cu_3Sn IMC. Secondly, it is suggested that a low temperature ramp rate at the beginning of the bonding process potentially improves the integrity of the bonded interconnects.

3.2 Outlook

Further development and characterization of Cu-Sn SLID bonding for the application of 3D heterogeneous integration can be continued from the listed point of view.

Firstly, it will be very interesting and beneficial to apply the interconnection technique developed in this thesis to stack MEMS structure and ASIC, where sealing and interconnection are achieved at the same step. Removing one temperature cycle out of the process flow can greatly reduce the production cost.

Secondly, though the reliability of the bonded interconnect was discussed in this work, a concrete reliability evaluation is valuable for interconnect bonded at various conditions, such as temperature ramp rate and flux.

Thirdly, a deeper understanding of the IMC formation mechanism is still desired. The influence of Cu grain size, purity of the electroplated metal on the IMC formation rate and bond integrity can be further investigated. Through literature study, it has been observed that massive work has been carried out regarding the Cu-Sn binary system. Most of these demonstrations are focused on the importance of this metal system with regards to Sn based solder reaction with Cu pad. It is equally important to investigate from a Cu-Sn SLID bonding point of view, i.e. the scenarios when Sn is fully reacted to become Cu-Sn IMC.

4 References

1. Taklo, M.M.V., et al. *3D stacked MEMS and ICs in a miniaturized sensor node*. in *Design, Test, Integration & Packaging of MEMS/MOEMS, 2009. MEMS/MOEMS '09. Symposium on*. 2009.

2. Marenco, N., *Downscaled assembly of vertically interconnected devices. Publishable final activity report.* 2009: on-line: http://www.isit.fraunhofer.de/german/modulint/david.html

3. Naitoh, Y., M. Horikawa, and T. Shimizu, *New Nonvolatile Memory Effect Showing Reproducible Large Resistance Ratio Employing Nano-gap Gold Junction.* , in *MRS Proceedings*. 2007. p. 0997-I04-08.

4. Taibi, R., et al. *Full characterization of Cu/Cu direct bonding for 3D integration*. in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*. 2010.

5. Ghosh, S. and M. Bayoumi. *On integrated CMOS-MEMS system-on-chip*. in *IEEE-NEWCAS Conference, 2005. The 3rd International*. 2005.

6. Brand, O., *1.15 - Packaging*, in *Comprehensive Microsystems*, Z. Hans, Editor. 2008, Elsevier: Oxford. p. 431-463.

7. Ristic, L. *Sensor fusion and MEMS for 10-DoF solutions*. 2012 [cited 2013; Available from: http://eetimes.com/design/medical-design/4395167/Sensor-fusion-and-MEMS-technology-for-10-DoF-solutions?pageNumber=1.

8. Kahn, J.M., R.H. Katz, and K.S.J. Pister, *Emerging Challenges: Mobile Networking for Smart Dust.* Journal Of Communications And Networks, 2000. **2**(3): p. 188-196.

9. Warneke, B., et al., *Smart Dust: communicating with a cubic-millimeter computer.* Computer, 2001. **34**(1): p. 44-51.

10. Pister, K. *SMART DUST:Autonomous sensing and communication in a cubic millimeter*. 2001; Available from: http://robotics.eecs.berkeley.edu/~pister/SmartDust/.

11. Available from: http://www.ecubes.org

12. Ramm, P. and A. Klumpp. *Through-Silicon Via Technologies for Extreme Miniaturized 3D Integrated Wireless Sensor Systems (e-CUBES)*. in *Interconnect Technology Conference, 2008. IITC 2008. International*. 2008.

13. Schjølberg-Henriksen, K., et al., *Miniaturised Sensor Node for Tire Pressure Monitoring (e-CUBES)*, in *Advanced Microsystems for Automotive Applications 2009*, G. Meyer, J. Valldorf, and W. Gessner, Editors. 2009, Springer Berlin Heidelberg. p. 313-331.

14. Ramm, P., et al. *3D integration technologies*. in *Design, Test, Integration & Packaging of MEMS/MOEMS, 2009. MEMS/MOEMS '09. Symposium on*. 2009.

15. Ramm, P., A. Klumpp, and J. Weber. *3D integration technologies for MEMS/IC systems*. in *Bipolar/BiCMOS Circuits and Technology Meeting, 2009. BCTM 2009. IEEE*. 2009.

16. Marenco, N., S. Warnat, and W. Reinert, *Interconnect Challenges in Highly Integrated MEMS/ASIC Subsystems.* Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP), 2007.

17. *The e-BRAINS project*. 2012 [cited 2013 May,13rd]; Available from: http://www.e-brains.org/.

18. Nasiri, S., *New innovations in MEMS fabrications are responsible for meeting the demand for low-cost inertial sensors for consumer markets, Available:http://www.invensense.com*.

19. *InvenSense IDG-300 dual-axis angular rate gyroscope sensor*, in *MEMS Process Review Report*. 2007: Ottawa.

20. [cited 2013 01.01]; Available from: http://www.yole.fr/.

21. [cited 2013 01 01]; Available from: http://www.i-micronews.com.

22. Dang, B., et al., *3D chip stacking with C4 technology.* IBM Journal of Research and Development, 2008. **52**(6): p. 599-609.

23. Mei, L., W.M. Lau, and Y. Jun, *On-demand multi-batch self-assembly of hybrid MEMS by patterning solders of different melting points.* Journal of Micromechanics and Microengineering, 2007. **17**(11): p. 2163.

24. Alam, S.M., et al. *Inter-Strata Connection Characteristics and Signal Transmission in Three-Dimensional (3D) Integration Technology*. in *Quality Electronic Design, 2007. ISQED '07. 8th International Symposium on*. 2007.

25. Tollefsen, T., et al., *Au-Sn SLID Bonding—Properties and Possibilities.* Metallurgical and Materials Transactions B, 2012. **43**(2): p. 397-405.

26. Chen, K.N., et al., *Copper bonded layers analysis and effects of copper surface conditions on bonding quality for three-dimensional integration.* Journal of Electronic Materials, 2005. **34**(12): p. 1464-1467.

27. Ko, C.-T. and K.-N. Chen, *Wafer-level bonding/stacking technology for 3D integration.* Microelectronics Reliability, 2010. **50**(4): p. 481-488.

28. Huffman, A., et al. *Effects of assembly process parameters on the structure and thermal stability of Sn-capped Cu bump bonds*. in *Electronic Components and Technology Conference, 2007. ECTC '07. Proceedings. 57th*. 2007.

29. Huffman, A., et al., *Fabrication and Characterization of Metal-to-metal Interconnect Structures for 3-D Integration.* Journal of Instrumentation, 2009(Issue 4): p. 03006.

30. Huebner, H., et al., *Face-to-face chip integration with full metal interface.* Advanced Metallisation Conference 2002 (AMC 2002), 2002. **18**: p. 53-58.

31. Du, M., W. Xu, and L. Luo. *Exploration of a new wafer-level hermetic sealing method by Cu/Sn isothermal solidification technique for MEMS/NEMS devices*. in *Micro- and Nanotechnology: Materials, Processes, Packaging, and Systems II*. 2005. Sydney, Australia: SPIE.

32. Kang, J.S., et al., *Isothermal solidification of Cu/Sn diffusion couples to form thin-solder joints.* Journal of Electronic Materials, 2002. **31**(11): p. 1238-1243.

33. Agarwal, R., et al. *Cu/Sn microbumps interconnect for 3D TSV chip stacking*. in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*. 2010.

34. Bosco, N.S. and F.W. Zok, *Critical interlayer thickness for transient liquid phase bonding in the Cu-Sn system.* Acta Materialia, 2004. **52**(10): p. 2965-2972.

35. Johnson, R.W., et al., *Power Device Packaging Technologies for Extreme Environments.* Electronics Packaging Manufacturing, IEEE Transactions on, 2007. **30**(3): p. 182-193.

36. Bernstien, L., *Semiconductor Joining by the Solid - Liquid - Interdiffusion (SLID) Process I . The Systems Ag - In, Au - In, and Cu - In*, in *J. Electrochem. Soc.* 1966. p. 1282-1288.

37. Huebner, H., et al., *Microcontacts with sub-30 [mu]m pitch for 3D chip-on-chip integration.* Microelectronic Engineering, 2006. **83**(11-12): p. 2155-2162.

38. Al-Sarawi, S.F., D. Abbott, and P.D. Franzon, *A review of 3-D packaging technology.* Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on, 1998. **21**(1): p. 2-14.

39. Hoivik, N., et al., *Fluxless wafer-level Cu-Sn bonding for Micro- and Nanosystems packaging.* Electronics System Integration Technology Conference, 2010.

40. Lapadatu, A., et al., *High-performance long wave infrared bolometer fabricated by wafer bonding.* 2010: p. 766016-766016.

41. Lapadatu, A., et al., *Cu-Sn Wafer Level Bonding for Vacuum Encapsulation of Microbolometer Focal Plane Arrays.* ECS Transactions, 2010. **33**(4): p. 73-82.

42. Duan, A., K. Aasmundtveit, and N. Hoivik. *Ultra-low leak detection of Cu-Sn SLID for high density wafer level packaging*. in *Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2011 12th International Conference on*. 2011.

43. Duan, A., et al., *Characterization of wafer-level bonded hermetic packages using optical leak detection.* Proc. SPIE 7381, 2009. **73811Y**.

44. Saunders, N. and A.P. Miodownik, *The Cu-Sn (Copper-Tin) system.* Bulletin of Alloy Phase Diagrams, 1990. **11**(3): p. 278-287.

45. Bosco, N.S. and F.W. Zok, *Strength of joints produced by transient liquid phase bonding in the Cu-Sn system.* Acta Materialia, 2005. **53**(7): p. 2019-2027.

46. Hoivik, N. and K. Aasmundtveit, *Wafer-Level SLID Bonding*, in *Handbook of Wafer Bonding*, P. Ramm, J.J.-Q. Lu, and M.M.V. Taklo, Editors. 2012, Wiley-VCH.

47. Tu, K.N., *Interdiffusion and reaction in bimetallic Cu-Sn thin films.* Acta Metallurgica, 1973. **21**(4): p. 347-354.

48. Song, J.Y., J. Yu, and T.Y. Lee, *Effects of reactive diffusion on stress evolution in Cu-Sn films.* Scripta Materialia, 2004. **51**(2): p. 167-170.

49. R.N.Wenzel, *Resistance of Solid Surfaces to Wetting by Water.* Ind,Eng,Chem, 1936. **28**: p. 988-994.

50. Su, P., et al., *The effects of underfill on the reliability of flip chip solder joints.* Journal of Electronic Materials, 1999. **28**(9): p. 1017-1022.

51. Ho, P.S., Z.P. Xiong, and K.H. Chua. *Study on Factors Affecting Underfill Flow and Underfill Voids in a Large-die Flip Chip Ball Grid*

Array (FCBGA) Package. in *Electronics Packaging Technology Conference, 2007. EPTC 2007. 9th*. 2007.

52. Sham, M.L. and K. Jang-Kyo. *Effects of flux residue and thermomechanical stresses on delamination failure in flip chip packages*. in *Electronic Materials and Packaging, 2000. (EMAP 2000). International Symposium on*. 2000.

53. Todd, M. *Effects of no-clean flux residue on the performance of flip-chip devices*. in *Advanced Packaging Materials: Processes, Properties andInterfaces, 2000. Proceedings. International Symposium on*. 2000.

54. Fan, Z., et al., *An investigation into the effects of flux residues on properties of underfill materials for flip chip packages.* Components and Packaging Technologies, IEEE Transactions on, 2003. **26**(1): p. 233-238.

55. Wen-Hao, L., et al. *Flux study for ultra fine pitch flip chip packages*. in *Microsystems, Packaging, Assembly and Circuits Technology Conference, 2009. IMPACT 2009. 4th International*. 2009.

Article I-V

I

Uniformity Requirements for Electroplated Cu-Sn Interconnects Used in Heterogeneous 3-D MEMS/ASIC Stacks

H. Liu, E. M. Husa, Z. Ramic, A. Munding, K. Aasmundtveit and N. Hoivik

Vestfold University College, Faculty of Science and Engineering,

Postbox 2243, N-3103 Tønsberg, Norway

Phone: +47 33037740, Fax: +47 33031100 E-mail: He.Liu@hive.no

Abstract

Interconnects play a crucial role for successful 3D-integration of MEMS with IC systems to create a System in a Package (SiP). Particularly, for non-reflow bonding processes the height uniformity of the interconnects will affect the bond quality and yield significantly. For 3D MEMS/ASIC heterogeneous integration, a sealing ring is usually required in conjunction with interconnects, which makes the uniformity of the deposited metal even more critical. Moreover, experiments showed that for patterns with a variety of features, areas with a low mask opening density are plated faster than areas with a high opening density. This will bring difficulties to 3D MEMS/ASIC integration, because during electroplating the sealing-ring and interconnects may have different deposition rates due to their pattern difference. In this work, the dependency of the uniformity of the electroplated micro-bumps on the plating geometry is investigated. An optimized electroplating mask was designed, and more uniform bumps were obtained. The optimized mask resulted in a variation of 13% across the chip, while 33% of variation was observed using a non-optimized mask. Analysis of the electroplated interconnect bumps using the optimized mask are expected to demonstrate sufficient uniformity to achieve bonding.

Key words: Electroplating, interconnects, uniformity, micro-bumps, SiP, MEMS.

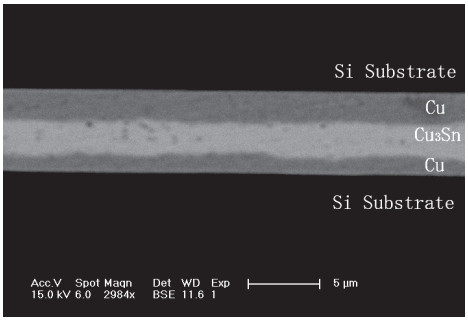


Figure 1: SEM backscattering image of a cross-section of a SLID-bonded sample. The light gray section in the center consists of the intermetallic compound Cu_3Sn.

Introduction

3-D stacking is the new trend for MEMS packaging and offers direct integration with IC systems [1, 2]. Compared to more conventional, discrete integration and packaging approaches, 3-D stacking can minimize the size of the final system, while improve the MEMS device performance at the same time.

In this work, Cu/Sn solid liquid interdiffusion (SLID) [3, 4] is chosen as the interconnection method [5, 6] where Cu and Sn thin films interdiffuse at a processing temperatures above the melting point of Sn (232^{o}C), solidifying the bond interface. The resulting Cu/Sn intermetallic compounds have a higher melting point (675^{o}C) [7] than the process temperature (280^{o}C). Figure 1 shows a cross-section of a bonded SLID joint which consists of Cu and the intermetallic phase Cu_3Sn. After the diffusion process is completed, and no pure Sn is left in the metal system, thus the joint can tolerate high temperatures. This allows for the packaged stack to undergo further processing, such as PCB attach, without compromising the first-level interconnects.

To facilitate relatively thick interconnects (a few microns), electroplating [5, 6] is chosen as the deposition method for the two metals. During the electroplating process, ensuring planarity of the electroplated bumps is critical for the bonding process to follow. One major difference of SLID to standard soldering process is that no reflow of metals is possible: one of the two metals, Cu, remains in its solid state, so if the non-planarity of

electroplated Cu across the die is significant, it will affect the bonding yield. This article will discuss issues concerning the plating uniformity and solutions are proposed.

The main reason for variations in bump height is a non-uniform current distribution across the wafer during electroplating. Usually, bumps located at the periphery of the wafer are higher than in the center due to increased current density at the wafer edge. However, the local current distribution also depends on the local area of openings in the plating mask. Thus, the height of an interconnect can also depend on its proximity to local structures, such as sealing rings, bump patterns on neighboring dies or other larger geometries (for MEMS/ASIC heterogeneous systems, a sealing ring is usually required [2]). Small patterns, such as dicing marks, alignment marks, or wires between bumps are usually plated faster. Thus, the design of a plating mask should be carefully considered to obtain a uniform electroplated bump height across the wafer, especially for wafer-level bonding and packaging.

Experiments

The Cu bumps was plated using a sulfuric electrolyte at room temperature with a DC power supply. The input current density was 10 mA/cm^2. In the plating bath, there was a continuous flow of the liquid together with movement of the wafer to achieve uniformity in the solution. Before plating, a 500 nm thick Au layer was sputtered on the wafer as a plating seed layer. After that, a photoresist layer was patterned using Shipley 1828 G2, so Cu can grow on specified areas.

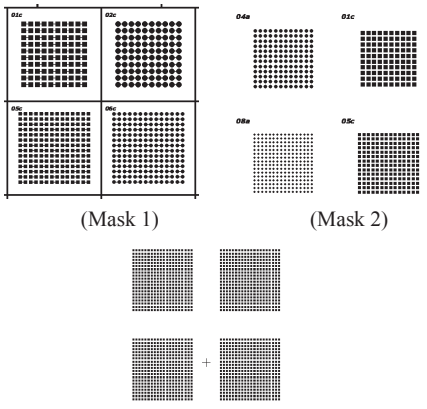


Figure 2: Layout of the three masks used for the evaluation of the electroplating process. Each mask consists of various test features to explore the electroplated bump uniformity of each experiment.

Three electroplating masks were used during the experiment. The layout of the three masks is shown in Figure 2, where Mask 1 consists of cells with daisy-chains of different bump size and number of interconnects. Other geometries, such as dicing marks and wires, are also included in the mask. In Mask 2 the small patterns are omitted, so this mask only comprises of bump arrays with different size. Mask 3 consists of arrays of identical bumps of the size 100 µm x 100 µm. A ring-like opening was incorporated with mask 2 and 3 which acts as a "current thief" in order to homogenize the current density at the edge of the wafer. The plating thickness for each plating experiment varied from 1.5 µm to 5.5 µm. As a figure of uniformity, the ratio of the maximum variation across the chip compared to the minimum height was calculated and evaluated. After photoresist stripping, the plated bump height was measured by a WYKO NT9100 white-light interferometer.

Results and discussion

For a chip with an electroplated bump array using mask 1, the measured height variation across the chip is shown in Figure 3, where the peripheral bumps on the chip are higher than the bumps in the center due to a non-uniform current distribution across the chip. The neighboring chip on the right hand side of this measured chip (which is not included in the figure) had a considerably smaller plating area (mask open area density = 19%) compared to the neighboring chip on the left hand side (mask open area density = 27%). Hence, the current density on the right part of the chip is higher and results in higher bumps on the right portion of

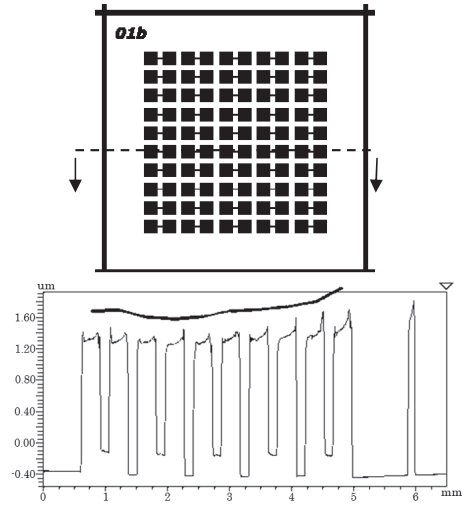


Figure 3: Measurement of electroplated Cu bump height. The plating mask used was mask 1; the line on top is a fit of the average bump height.

the chip. As shown in Table 1, the bump with the smallest height is located at the centre of the chip and was measured to be 1.6 µm high, and the peripheral bumps are higher (1.7 µm and 1.8 µm). In this case, peripheral bumps at the right of the chip were observed to be the highest, due to the fact that the neighboring chip to the right has a lower opening density than the one to the left. From the measurement, an edge effect (spikes seen at the edges of the bumps) of electroplating is also observed, which additionally contributes to the plating non-planarity. However, this is assumed to be the result of a different phenomenon, which will be addressed in future investigations, hence will not be the focus of this article. The small features on this chip, such as dicing marks and wires, are observed to be higher than the interconnect bumps, and their heights are summarized in Table 1.

Table 1: Measured bump height variation on one chip using Mask 1. (Unit: µm)

Lowest bump	Highest bump	Dicing marks	Wires (Centre)
1.6	1.8(right),1.7(left)	2.0	1.8

Table 2: Measured bump height variation between chips with different opening density, using mask 2.

Chip No.	Bump size	Number of bumps	Opening density	Average height
1	310µm x310µm	10x10	24.8%	3.55µm
2	350µm DIA	10x10	24.8%	3.31µm
3	282µm DIA	12x12	13.3%	3.59µm
4	160µm x160µm	16x16	9.73%	4.10µm
5	110µm x110µm	18x18	5.94%	5.46µm
6	40µm x40µm	26x26	2.94%	5.00µm

The second mask was accommodated from the first one by omitting all the small features from the mask except for the interconnect bumps. This mask consists of bump arrays with different sizes and numbers of interconnects, and the plating results show that in each chip the metal deposition rate is different due to the variation of the opening density. The height variation of bumps on different chips is summarized in Table 2, where the opening density represents the ratio between the area of the mask opening to the total area of the chip. From the data, it is observed that the chips with a small opening density tend to have a higher metal deposition rate. However, due to the fact that each chip has neighboring chips with different opening area, there is some height variation, even when the chips have the same opening density (chip No. 1 and chip No. 2). Thus, it is difficult to evaluate the relationship between the opening density and the plating rate at this point.

Using mask 3, which is more uniform than the other two, a more uniform bump height was obtained, as shown in Figure 4. For electroplating using mask 1 and 3, the plating time was set to be different, resulting in a different average bump height. As a figure of uniformity, the ratio between the height variation compared to the lowest bump height is shown in Table 4. Using mask 3, the height variation within one chip was reduced to 13%, whereas with mask 1, the variation was 33%. However, peripheral bumps were still observed to be higher. The height variation is acceptable for this application, because Sn will be plated on top of the Cu bumps, and during the bonding process the Sn layer will melt and compensate for small height variations in the Cu bumps. If the Sn layer is thick enough to compensate the height variation of plated Cu from both sides, a successful bond can be expected. In Cu/Sn SLID bonding, a minimum thickness ratio of Cu:Sn=1.3:1 is required in order to supply enough Cu to reach a complete formation of Cu_3Sn, which is the favored intermetallic phase due to its improved mechanical performance and chemical stability over other intermetallic phases. Excess Cu is usually preferred in order to ensure that no Sn or another intermetallic phase, such as Cu_6Sn_5, remains in the joint interface. For example, if the plated metal system has a thickness ratio of Cu:Sn=5:3, the maximum height variation that the Sn layer can possibly tolerate is 60% of the total thickness of Cu. In this manner, both plating results using mask 1 (33%) and mask3 (13%) are expected to achieve successful bonds. However, with more uniformly plated Cu bumps, the critical Sn layer thickness to achieve bonds is reduced, which makes the process more flexible.

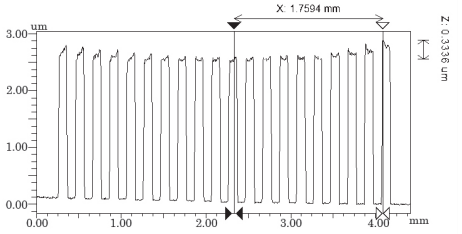


Figure 4: Measurement of Cu bump height using mask 3. A homogeneous interconnect height distribution is obtained by ensuring a uniform mask opening density. The maximum variation within one chip was 0.33 µm with a bump height of 2.5 µm.

Mask 3 can further be optimized. For example, if the distance between the bump arrays is decreased, the electric field can be more uniform, and the height variation can be reduced. Alternatively, a sacrificial ring-like opening can be

put around the bump array, to obtain a more uniform electric field.

Table 3: Measured electroplated interconnect height variation across chip using mask 1 and mask 3.

	Mask 1	Mask 3
Min	1.5µm	2.5µm
Max-Min	0.45µm	0.33µm
(Max-Min)/Min	33%	13%

Furthermore, in the third mask, a ring was incorporated at the edge of the wafer to resolve the problem of excess plating at the peripheral area of the wafer. In this case, the effect of the ring is excessive so the bumps near the ring were observed to be lower, as shown in Figure 5. This supports the argument that the mask design should be optimized to find a suitable ring size to accomplish uniform plating at the peripheral area of the wafer.

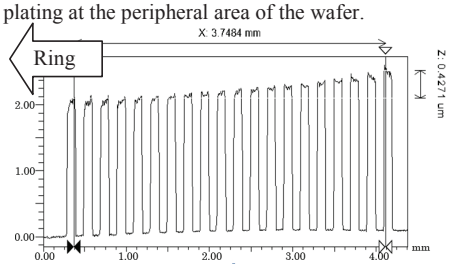


Figure 5: Measured bump height of one chip close to the sacrificial ring on the edge of the wafer. Mask 3 was used as the plating mask.

From the above experiments, it can be concluded that the plating rate of one area opening is not only affected by the area itself, but also influenced by its neighbors, because the adjacent patterns also play a role in distributing the electric field. The geometry of the openings determines how the electric field distributes in the electrolyte and further determines the current density at the open areas. The desired current density of this series of plating experiments was 10 mA/cm^2 and the current density was multiplied by the total open areas on the wafer to get the input current. However, due to the inhomogeneous distribution of the current, the actual current density is lower in some areas and higher in others, resulting in a different plating rate.

Currently a simulation tool is under development for predicting these variations of the plating rate across the wafer. This will enable an optimization of plating mask geometries.

Concluding remarks

The electroplating process in micro fabrication is very sensitive to the actual geometry to be plated. Areas with different opening densities will give rise to different plating rates on the wafer. For 3D heterogeneous MEMS/ASIC integration, in addition to the interconnects, a sealing ring is usually required, which will lead to undesired variations in overall height uniformity of the interconnects. Therefore, design rules for electroplating mask design must be established which consider the influence of geometries in order to reduce any height variation. For the application of a non-reflow bonding process with hermetic sealing requirements, the plating uniformity is particularly critical. An optimized plating mask will have a uniform opening density across the wafer, and include an additional sacrificial ring opening at the periphery of the wafer. Furthermore, small patterns are not preferred in a mask design, especially if they are isolated. Therefore, for successful 3D MEMS/ASIC heterogeneous integration, the interconnect bumps may have a lower pattern density than the sealing ring, thus some sacrificial pattern should be put near/around the interconnects to achieve a uniform electric field.

By using an optimized plating mask, the height variation of plated interconnect bumps is significantly reduced to 13%, while a non-uniform mask resulted in 33% bump height variation. The plated Cu bumps with the optimized mask are considered to be acceptable for SLID bonding.

References

[1] S. Stoukatch, C. Winters, E. Beyne, W. De Raedt, and V. Hoof, "3D-SIP integration for autonomous sensor nodes," *Proceedings of the 56th Electronic Components and Technology Conference. IEEE,* pp. 404-408, 2006.

[2] N. Marenco, S. Warnat, and W. Reinert, "Interconnect Challenges in Highly Integrated MEMS/ASIC Subsystems," *Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP),* 2007.

[3] K. N. Tu, "Interdiffusion and reaction in bimetallic Cu-Sn thin films," *Acta Metallurgica,* vol. 21, pp. 347-354, 1973.

[4] R. A. Gagliano and M. E. Fine, "Thickening kinetics of interfacial Cu6Sn5 and Cu3Sn layers during reaction of liquid tin with solid copper," *Journal of Electronic Materials,* vol. 32, pp. 1441-1447, Dec 2003.

[5] H. Huebner, S. Penka, B. Barchmann, M. Eigner, W. Gruber, M. Nobis, S. Janka, G. Kristen, and M. Schneegans, "Microcontacts with sub-30 [mu]m pitch for 3D chip-on-chip integration," *Microelectronic Engineering,* vol. 83, pp. 2155-2162, 2006.

[6] H. Huebner, O. Ehrmann, M. Eigner, W. Gruber, A. Klumpp, R. Merkel, P. Ramm, M. Roth, J. Weber, and R. Wieland, "Face-to-Face Chip Integration with Full Metal Interface," *Advanced Metallisation Conference 2002 (AMC 2002),* vol. 18, pp. 53-58, 2002.

[7] F. Bartels, J. W. Morris, G. Dalke, and W. Gust, "Intermetallic Phase-Formation in Thin Solid-Liquid Diffusion Couples," *Journal of Electronic Materials,* vol. 23, pp. 787-790, Aug 1994.

II

III

High-Temperature Stable Au-Sn and Cu-Sn Interconnects for 3D Stacked Applications

Advanced Processes and Materials – I

Nils Hoivik, He Liu, Kaiying Wang, Guttorm Salomonsen and Knut Aasmundtveit

Institute of Microsystems Technology, Vestfold University College, Norway

Abstract. The desire to directly integrate MEMS with ASICs in a 3D stack is the main motivation behind the development of a bonding technology suitable for both interconnects and seal rings. SLID (Solid-Liquid Inter-Diffusion) bonding processes based upon Au-Sn and Cu-Sn (high melting point metal/low melting point metal) are therefore investigated. SLID bonding allows for repeated high temperature processing cycles as in the case for chip stacking, or for interconnections and seal rings bonded at different process steps. This work describes results obtained for fluxless bonding of SLID Au-Sn and Cu-Sn interconnects and seal rings, where a thin layer of intermetallic compound (IMC) on the Cu or Sn surface protects the metal surfaces from oxidizing at elevated temperatures. To evaluate the bond strength, test dies bonded at various temperatures were subjected to SEM/EDX bond line analysis, and shear testing at both room- and elevated temperatures. Au-Sn samples bonded at 280 ^{o}C re-melt at elevated temperatures; whereas samples bonded at 350 ^{o}C remain intact past the initial bonding temperature. For the Cu-Sn samples, the measured shear strength is comparable to conventionally bonded interconnects. In order to remain within the uniformity requirements for SLID bonding, the pattern density of electroplated interconnects and seal rings require an optimized layout which can be calculated based upon the effective area.

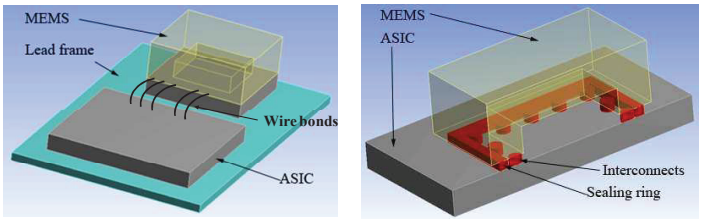
Keywords: MEMS, 3D integration, wafer level packaging, SLID bonding, wafer bonding

1 Introduction

The recent advances within 3D IC integration and packaging to create a system in a package (SIP) have become a main driving factor for miniaturization and integration of future MEMS-based sensor systems. The desire to directly integrate MEMS with ASICs in a 3D stack is the main motivation behind the devel-

opment of a bonding technology which is suitable for both interconnects and seal rings. For a MEMS-based SIP, the performance, or sensing functionalities, may be improved without increasing the overall size. Since, in a 3D package the sensor die, ASIC, and passives are stacked in the third dimension which reduces the size of the final product and shorten the signal path between the individual parts [1], [2]. The stacked approach also enables high I/O density, if required, which reduces cost and allows for optimization of the MEMS sensor performance. Furthermore, to combine the stacking process with the cavity sealing process is becoming realistic, i.e., one can make the electrical connection, mechanical attachment, and cavity sealing process within a single chip stacking step, as illustrated in Figure 1. Traditionally, the final processing step in MEMS fabrication is hermetic sealing of the fragile devices, followed by dicing. The ASIC and MEMS devices are then mounted in a 2D package and interconnected using wire bonds, as shown in Figure 1a. 3D integration and packaging enables an appealing alternative since MEMS devices may be directly sealed during bonding to the ASIC, in one process step, as shown in Figure 1b, where they combined create a complete package.

Correct packaging and integration techniques for microsystem devices are crucial to ensure reliable MEMS devices. It is worth mentioning that packaging of microsystems, in particular the hermeticity requirements, significantly increase the total cost of a final product. Therefore, with 3D stacking and direct sealing, time and cost can be saved, and performance of the product can be improved.



(a) (b)

Figure 1: Illustration of (a) traditional microsystem package with discrete devices mounted on a lead frame and (b) sealed and interconnected microsystem where the ASIC and MEMS combined creates a complete package.

Hermetic sealing combined with interconnects which are stable at elevated temperatures is important for several applications, such as automotive applications, engine or combustion control, oil and gas extraction to mention a few. High temperatures may also be experienced during subsequent processing of the bonded parts, for example getter activation for high-vacuum cavities. These getters typically require an activation temperature of 350 ^{o}C, or higher, which poses a challenge to the bond integrity. Other examples include dies which are to be stacked and bonded to a substrate in subsequent processing steps. Thus, the bonds need to be stable at higher temperatures than the initial bonding temperature, so that the initial bonds do not melt when the bonding process is repeated.

2 Cu-Sn and Au-Sn SLID Bonding

In this project, bonding techniques using Solid Liquid Inter-Diffusion (SLID) with Cu or Au together with Sn have been studied [1]-[8]. The benefit of these metallurgies is that a bond will initially form at the melting point of Sn (232 ^{o}C), whereas the final intermetallic compound (IMC) Au_xSn_y and Cu_xSn_y will have a higher melting point. This allows for subsequent bonding cycles in the case of chip stacking, or bonding of interconnections and seal rings at different fabrication steps. The non-eutectic intermetallic compound (Cu_3Sn) has a melting point at 676°C, whereas the eutectic Au-Sn (80 wt% Au) alloy melts at 278 °C. Since the eutectic Au-Sn composition has a relatively low melting/re-melting temperature we will attempt to target Au-rich intermetallic compounds, which have higher melting points than the eutectic composition. Thus once the joint is made, it can stand fairly high temperature during the succeeding process, such as molding, 2nd-level packaging, etc. Compared to thermocompression bonding, such as Cu-to-Cu which requires temperatures as high as 400 °C, the bonding pressure and temperature used in SLID bonding is quite favorable in conjunction with sensitive MEMS devices. SLID bonding using Cu-Sn has been demonstrated without pressure applied to the two surfaces [3], which does however require intimate contact between all bonding partners. Furthermore, both the intermetallic Cu_3Sn and Au_xSn_x IMCs have been observed to be quite inert when exposed to humidity and moisture, so it is a good candidate material for both interconnects and hermetic seal rings [3]. Table 1 provides a comparison of common interconnect technologies demonstrated for 3D stacked applications.

Table 1: Comparison of metallic interconnect technologies demonstrated at wafer-level for 3D stacked applications.

Interconnect Technology	Process Temperature	Process Pressure	Fluxless	Topography requirements	3D stacking
Eutectic solder[#]	Low	Low	No	NA	No
Thermo compression*	Medium-High	High	Yes	nm	Yes
SLID	Medium	Low	Yes	µm	Yes

* Referring to Cu-Cu and Au-Au; [#] commonly used Sn-based Pb-free solders.

The Au-Sn and Cu-Sn phase diagrams are shown in Figure 2 and Figure 3, respectively. The Au-Sn phase diagram illustrates the complexity and the large number of intermetallic compounds (IMC) for this metallurgy. All of the phases have a higher melting point than pure Sn, and in particular the δ and the ζ/ζ' phases have a melting point above the eutectic composition at 419 ^{o}C and 521 ^{o}C, respectively. For applications where the bond is to resists higher temperature, either one of the IMCs may be appropriate. However, if there remains a surplus of Au in a bond after formation of an IMC, a bond made of the δ phase may be susceptible

to be converted to a eutectic, or near-eutectic, structure over time due to Au-Sn interdiffusion. This would lead to a bond-line with a lower melting point. However, a bond with the ζ/ζ' phases present is not expected to convert into lower-melting phases over time. It is noteworthy to point out that the eutectic composition does consist of both the δ and the ζ/ζ' phases present at the same time at a ratio corresponding to 80%wt Au and 20%wt Sn.

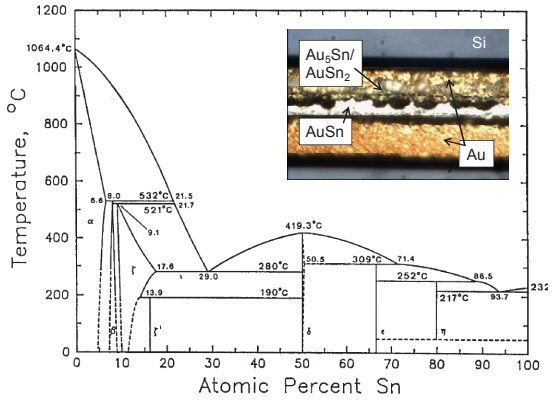


Figure 2: Au-Sn phase diagram. The insert illustrates a sample bond line with various phases present between pure Au (phase diagram adapted from [4]).

Compared to Au-Sn IMC bond lines, which may be rather complex and form various phases, Cu-Sn SLID interconnects initially form two distinct phases: η-Cu_6Sn_5 and ε-Cu_3Sn.With reference to the Cu-Sn phase diagram shown in Figure 3, at a bonding temperature above the melting point of Sn (232 °C) interdiffusion processes form these two phases. At first, the molten Sn starts to dissolve Cu and the first IMC η-phase which is meta-stable, is formed. This particular phase actually forms even at room temperature; however no other phases are formed unless the temperature is elevated [10]. Upon complete transformation of all available Sn to the η-phase, the second IMC ε-phase (Cu_3Sn) is formed when the η-phase reacts with Cu. The insert in Figure 3 shows a SEM cross-section images of a bonded sample where both the ε- and η-phases are present in the bond line. The IMC formation process will terminate upon complete transformation of all IMCs to the stable Cu_3Sn ε-phase, which will suppress any further phase growth, even at elevated temperatures up to 676 °C.

The benefit of SLID bonding for interconnects, and especially for 3D applications is quite apparent. With interconnects or bond lines stable for a large temperature variation, subsequent bonding steps, processing at elevated temperatures, or thermal annealing to for instance activate getter materials, will not compromise the initial bonds and integrity of the package.

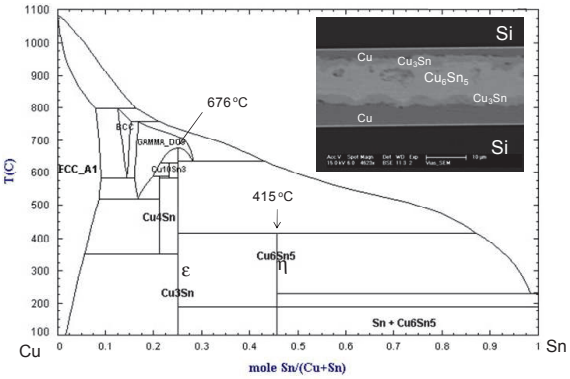


Figure 3: Cu-Sn phase diagram [9]. The insert illustrates a bond-line with both the ε and η-phase present. The IMC formation process will eventually terminate upon complete transformation to the stable ε-phase in the bond-line.

This work presents an alternate method to achieve fluxless bonding for SLID Au/Sn and Cu/Sn bonding processes by protecting the metal surfaces from oxidizing at elevated temperatures using a thin layer of IMC on the Cu or Sn surface. To evaluate the bond strength, test dies bonded to Au and Cu patterned substrates were subjected to SEM/EDX bond line analysis. Shear testing was performed at room temperature for Cu-Sn bonded dies and both room- and elevated temperatures for the Au-Sn samples.

3 Fabrication of Test Vehicles for Fluxless Bonding

For any metallic bonding to be successful, a key requirement is to remove, or prevent, any oxides on the surface of the material. Various fluxes have been used as critical process steps to ensure an oxide-free metallic surface, and any bonding process which can be done without this added process step is called fluxless or flux-free. In particular, Cu is prone to oxidation, which is accelerated at elevated temperatures. Since it is not self-passivating process, the oxide will continue to grow in thickness unless inhibited from forming. Sn oxides are somewhat easier to manage in SLID bonding as they are thinner than Cu oxides, and bonding is possible without active removal of this layer as some of the Sn oxides will be dissolved into the alloy. However, the Cu-Sn bonding process is performed after either an acid etch of the Cu oxide (with 5% HCl solution), or reduction using formic acid vapor in a nitrogen atmosphere. Both methods require a rinse step in DI water afterwards to remove any residual compounds. Bonding must also be

performed in an inert atmosphere, or in vacuum, to avoid any re-oxidation of the metal surfaces at elevated temperatures.

This work presents an approach to achieve fluxless bonding for SLID Au-Sn and Cu-Sn interconnects and seal-rings without wet pre-cleaning of the metal surfaces or bonding in vacuum. This is particularly important for wafers with released, and free-standing, MEMS devices where a wet pre-cleaning step is not compatible. Thus, in order to protect the metal surfaces from oxidizing at elevated temperatures a nm-thick sandwich-multilayer (100-200 nm) are electroplated on the interconnects and seal rings followed by a pre-bonding anneal process step to form a thin layer of IMC on the Cu or Sn surface [11],[12]. Earlier approaches have been successfully demonstrated for Sn-based soldering using Ag-Sn [13] and In-Ag [14]; however the Sn-rich solders are less stable at elevated temperatures. Another approach using Cu to cap the Sn layer to create Cu_6Sn_5 and Au to protect the Cu layer was demonstrated in [10]. However the final bond line will then consist of both Au-Sn IMCs and Cu_3Sn, and hydrogen atmosphere was required to shield the samples from any oxygen penetration during bonding.

3.1 Au-Sn

Fluxless bonding of Au-Sn electroplated layers (using a thin Au layer on top of Sn), with a resulting bondline of the IMC $AuSn_2$ was previously reported in [11]. The present work investigates the possibility to use Au-rich Au-Sn compounds for SLID-type bonding, with the ultimate goal of obtaining higher temperature stability. Oxidized (300 nm oxide) silicon wafers with sputtered TiW/Au adhesion/seed layers were purchased from Reinhardt Microtech AG, Switzerland. The thickness of the TiW adhesion layer is 60 nm, and the Au seed layer is 100 nm. These metalized wafers were patterned with photoresist AZ4562 for electroplating metallic layers in the shape of rectangular bonding frames. Gold electroplating was performed in gold cyanide solution at a temperature range of 60–65 ^{o}C, with a current density 5.4 mA/cm^2. Sn electroplating (on top of the gold layer) was deposited in a Sn sulphate-based solution at room temperature, with a current density 10 mA/cm$^{2.}$ Figure 4 illustrates the layered structures which were fabricated with a single Au layer: 4.0 µm and multilayer Au/Sn/Au: 4.0 µm/2.0 µm/0.1 µm, respectively.

None of the samples have exposed Sn, which will minimize the chance for any oxidation, and makes fluxless bonding possible. The layer structure of the samples gives an overall composition of 8 wt% Sn (13 at% Sn) which gives a surplus of Au relative to the eutectic point, and also a small surplus of Au relative to the ζ' phase (Au_5Sn).

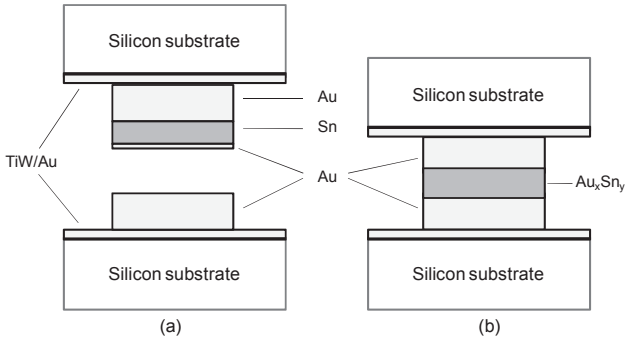


Figure 4: Schematic illustration of the (a) layered electroplated Au (4.0 µm) and Au (4.0 µm) / Sn (2.0 µm) / Au (0.1 µm) structures for fluxless SLID bonding. After bonding (b) the joint comprise of various IMC and Au.

Pairs of samples, consisting of one Au-layered chip and one Au/Sn/Au-layered chip were bonded. The bonding was carried out in two steps. First, a flip chip bonder (MAT-6400), was used for pick and place and pre-bond at room temperature in air (applying a force of 30 N for 30 seconds), then the positioned sample pair was SLID bonded, using a hotplate at 350 ^{o}C in a vacuum chamber at 5 mBar. Other samples were bonded directly on the flip-chip bonder in formic acid saturated nitrogen atmosphere at 280 ^{o}C. Samples were bonded using different bonding times (2 min, 10 min, 20 min and 30 min).

3.2 Cu-Sn

Similarly to the Au-Sn samples, the Cu-Sn test vehicles were fabricated by first electroplating Cu on oxidized Si wafers with sputtered TiW/Au and Ti/Au adhesion and seedlayers. The thickness of the adhesion layer was 100 nm and the Au seedlayer 500 nm. Photoresist AZ4562 was used to define the interconnect pattern. Ar+O_2 Plasma treatment was carried out before the plating process to ensure a clean seed layer surface. The Cu and Sn features were electroplated using a commercial Cu- and Sn sulphate-based solution at room temperature, with a current density of 10 mA/cm^2. Pulse-reverse current was applied to ensure good uniformity across the wafer. Figure 5 illustrates the fabricated interconnects with Cu (5.0 µm)/Sn (0.1 µm) and Cu (5.0 µm)/Sn (3.0 µm) structures for fluxless Cu-Sn SLID bonding.

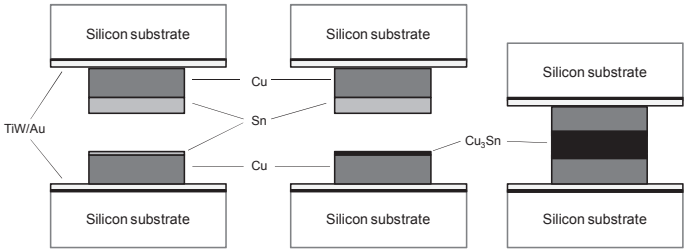


Figure 5: Schematic illustration of (a) layered Cu/Sn structures with Cu (5.0 µm)/Sn (0.1 µm) and Cu (5.0 µm)/Sn (3.0 µm) structures for fluxless SLID bonding. (b) The thin Sn layer is then converted to ε-phase Cu_3Sn by annealing, and (c) bonded to create a single phase IMC/Cu interconnects.

The technique of using an intermediate layer to protect the Cu layer from oxidizing is not new, and has been demonstrated earlier using Au, as well as allowing a thin Sn layer of Cu_6Sn_5 form on the Cu surface [10]. However, it has been determined that the corrosion behavior of Cu_6Sn_5 is almost as corrosive as pure Cu, whereas the stable Cu_3Sn phase is completely inert for the same test conditions [3]. Therefore, a very important annealing step is introduced (as shown in Figure 5b) to ensure that the IMC is completely converted to ε-phase Cu_3Sn. This is done in vacuum (2 mBar) at 250 ^oC for 5 minutes. The ability of Cu_3Sn to protect the Cu from oxidation was further verified by electroplating a 0.1-0.2 um thin Sn layer on a 4.0 um thick Cu layer which was annealed in vacuum to convert the top Sn layer to Cu_3Sn. The samples were then further annealed in ambient air at various temperatures and times, together with electroplated Cu films at the same conditions for verification. As expected, a large color change was observed on the Cu films due to oxidation, whereas the Cu_3Sn films retained the same color appearance. Both surfaces were then examined using EDX which identified a stable oxygen level in the Cu_3Sn film compared to the Cu samples.

Fluxless bonding of the Cu/Cu_3Sn to Cu/Sn dies was carried out on a MAT 6400 flip-chip machine in ambient atmosphere at 260 ^oC for 10 minutes with a pressure of 7 MPa. Same conditions were used for test dies using formic acid saturated nitrogen atmosphere. After bonding, the samples were removed from the hot bonding stage and allowed to naturally cool down to room temperature.

4 Results and Discussion

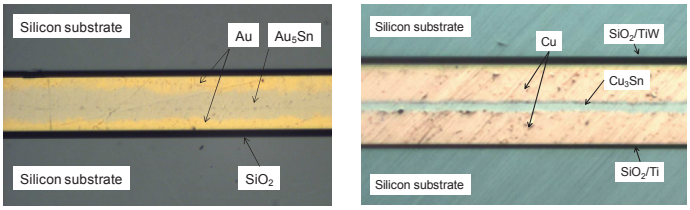
To evaluate the bond strength, test dies bonded to Au and Cu patterned substrates carried out at different conditions, such as temperature, pressure, flux,

etc. were subjected to SEM/EDX bond line analysis and shear testing at both room and elevated temperatures.

The bond strength at room temperature was characterized using standard die shear testing methods, using a Delvotec 5000. The test dies were diced into smaller pieces prior to die shear testing to permit the maximum force (50 N) to be sufficient to test the bond destructively. To determine the stability of bonded samples at elevated temperatures, two independent experiments were set up using a hot plate and an oven [12]. For the hot plate, the dies were positioned in a recess shallower than the die thickness and a shear force of around 2 N was applied to the top die. For the oven, dies were mounted in a fixture giving a constant shear force in the order of 5 N. These experiments were both designed to reveal any melting of the bonding layer since the top die would be pushed off if the bonding layer melts.

4.1 Bonding Results and Shear Strength

After bonding, samples were cut and polished for optical inspection and SEM/EDX verification of the various IMC phases present in the bond lines. Figure 6 shows two optical micrographs of the cross-sections of both metallurgies which were bonded. In both images the bond lines is seen to be uniform and appears as a grayish colored phase. For the Cu-Sn sample, the bond line is thinner than expected since the pressure was continuously applied during the bond cycle, whereas the Au-Sn sample was bonded without any pressure applied. The bond pressure applied affects the final bond line thickness since it squeezes out the liquid Sn from between the two bond pads.



(a) (b)

Figure 6: Optical micrographs of cross-sectioned bonded samples, (a) Au-Sn sample bonded at 350 ^{o}C for 2 minutes [12] and (b) Cu-Sn sample bonded at 260 ^{o}C for 10 minutes. The IMC compositions were verified using EDX inspection.

For the multilayered Au-Sn test dies bonded at 350 ^{o}C, the bond strength at room temperature for the sample with 10 minutes bonding time was measured to exceed 60 MPa, as compared to a shear strength of 11 MPa for samples bonded at 280 ^{o}C. This is a very high shear strength compared to previously reported val-

ues in the literature; however it is believed that the single-phase bond line obtained by bonding at 350 ^{o}C contributes to the increased strength. Further bonding experiments and analysis are in progress to evaluate this further. High-temperature integrity of the Au-Sn samples was evaluated by shear testing on a heated stage-with shear forces up to 2 N. Samples bonded at 280 ^{o}C did not survive testing at elevated temperatures, indicating that the Au-Sn IMC layer melted. However, samples bonded at 350 ^{o}C showed no delamination or movement of the uppermost chip within the temperature testing range. This is valid for all samples, independent of the bonding time, which indicates that bonding at higher temperatures shifts the IMC composition towards the Au-rich region of the phase diagram, as compared to samples bonded at lower temperatures which comprise of various, and more Sn-rich, IMC phases.

The strength of the multilayered Cu-Sn test dies were only tested at room temperature since both Cu-Sn IMC phases have higher melting points than 350 ^{o}C. Thus, conventional Cu-Sn SLID dies bonded using formic acid vapor flux was fabricated using the same conditions to offer a direct comparison. A total of eight pairs of test dies were bonded with a measured shear strength exceeding 9 MPa, which is the upper limit for the test system for the given interconnect area on the test dies. For conventional Cu-Sn/Cu test dies bonded with flux the measured shear strength range from 9 – 16 MPa. Table 2 presents a comparison of bond integrity of both metallurgies and bonding temperatures.

Table 2: Comparison of bond integrity of Au-Sn and Cu-Sn test dies bonded at various temperatures with and without flux.

	Au-Sn		Cu-Sn	
Flux	Yes	No	Yes	No
Bonding temperature	280 ^{o}C	350 ^{o}C	260 ^{o}C	260 ^{o}C
Shear strength at 20 ^{o}C	11 MPa	> 60 MPa	9-16MPa	> 9 MPa
Solid bond at 280 ^{o}C	No	Yes	--	--
Solid bond at 350 ^{o}C	No	Yes	--	--

4.2 Interconnect and bond frame uniformity requirements

One particular challenge to SLID bonding, and especially at wafer-level, is the lack of a collapsible or reflow process, thus the height uniformity of the electroplated features will significantly affect the bond quality and yield. As mentioned earlier, for many 3D MEMS/ASIC heterogeneous integration applications, a sealing ring is usually required in conjunction with interconnects, which makes the uniformity of the deposited metal thickness even more critical [2]. Electroplating process control together with pattern layout optimization is therefore crucial to increase the overall yield for wafer-level integration and packaging.

It is well known that smaller features (such as interconnects) often end up thicker than larger features (such as seal rings) when electroplated. Since there is a linear relationship between current density and electroplated thickness, the height of electroplated features can be estimated by simulating the variation of current densities in a mask [15]. Both seal rings and interconnects must be arranged with optimized areas, and pitch (p), as to minimize any height differences. Figure 7 shows the simulated height differences between interconnects and seal rings for an array of bumps with diameter ranging from 75 um to 250 um together with a seal ring 250 um wide. With an optimized pitch (equal pattern density), interconnects down to 100 µm in diameter can be used in conjunction with a 250 µm wide ring while still remaining within the permissible height variation for SLID bonding.

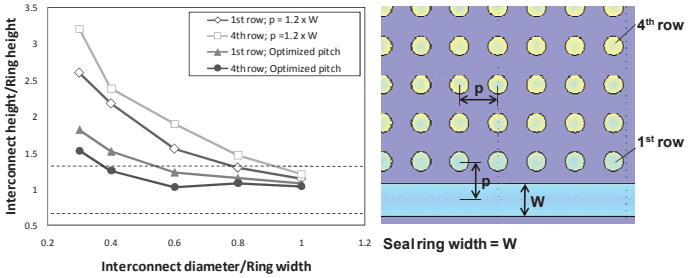


Figure 7: Simulated height variation for electroplated interconnects and seal ring as a function of bump diameter and pitch. The dashed lines represent permissible height variation for SLID bonding using 5 µm Cu and 3 µm thick Sn bonding features.

5 Summary

Technological advances within 3D IC integration and packaging continue to push miniaturization and integration of future MEMS-based sensor systems. Integrating MEMS with ASICs in a 3D stack requires a bonding technology suitable for both interconnects and seal rings. SLID bonding of Au-Sn and Cu-Sn which incorporates a 100-200 nm thick protective IMC layer to prevent oxidization of the surfaces at elevated temperatures is investigated. This is particularly important for wafers with released, and free-standing, MEMS devices where a wet pre-cleaning step is not compatible. It is important to keep the protective IMC layer intentionally thin as not to interfere with the inter-diffusion process during bonding. For bonded Cu-Sn samples, with a thin Cu_3Sn layer to protect the Cu surface, the measured shear strength is comparable to conventionally SLID bonded interconnects. For Au-Sn samples bonded at 350 ^{o}C, no bond delamination was observed up to 350 ^{o}C which is 70 ^{o}C higher than the eutectic point. Varying the bonding time (in the range of 2–30 minutes) does not have significant effect on the

result. The bonding structure is expected to be stable over time, and not to change composition due to interdiffusion of Au and Sn. The investigated bonding method therefore has potential for high-temperature applications and as a bonding method to tolerate high-temperature processes, such as chip stacking and getter activation, after bonding.

Acknowledgements

This project is funded by RCN BIA project No. 174320, "3DHMNS - 3D Heterogeneous Micro Nano Systems". The authors wish to thank Zekija Ramic, Ellen M. Husa and Tormod Vinsand at VUC for laboratory assistance.

References

[1] P. Ramm and A. Sauer, “3D integration technologies for ultrasmall wireless sensor systems - The e-Cubes project”, Future Fab International (2007), Nr. 23, pp 80-82.
[2] N. Marenco, S. Warnat and W. Reinert, “Interconnect Challenges in Highly Integrated MEMS/ASIC Subsystems”, Proceedings of DTIP 2007, Stresa Italy, 25-27 April, 2007.
[3] H. Huebner, S. Penka, B. Barchmann, M. Eigner, W. Gruber, M. Nobis, S. Janka, G. Kristen, and M. Schneegans, "Microcontacts with sub-30 [mu]m pitch for 3D chip-on-chip integration," Microelectronic Engineering, vol. 83, pp. 2155-2162, 2006.
[4] L. Yin a, S. J. Meschter b, T. J. Singler, “Wetting in the Au–Sn System”, Acta Materialia Vol. 52, pp. 2873–2888, 2004.
[5] R.S. Forman and G. Minogue, “The Basics of Wafer-Level AuSn Soldering,” Chip Scale Review, Vol. 8, pp. 55-59, 2004.
[6] C.C. Lee and C.Y. Wang, “A low temperature bonding process using deposited gold tin composites”, Thin Solid Films, 208, pp 202-209, 1992.
[7] D.Q. Yu, H. Oppermann, J. Kleff and M. Hutter, “Interfacial metallurgical reaction between small flip-chip Sn/Au bumps and thin film Au/TiW metallizatgion under multiple reflow”, Scripta Materials, 58, pp 606-609, 2008.
[8] L. Dietrich, G. Engelmann, O. Ehrmann and H. Reichl, “Gold and gold-tin wafer bumping by electrricchemical deposition for flip chip and TAB”, EuPac’98, Nürnberg, pp 28-31, 1998.
[9] FactSage Thermochemical Software and Databases - http://www.crct.polymtl.ca/fact/
[10] C.C. Lee and Y.C. Chen, “High temperature tin-copper joints produced at low process temperature for stress reduction”, Thin Solid Films, Vol. 286, pp 213-218, 1996.
[11] K. Wang, K. Aasmundtveit, and H. Jakobsen, "Surface Evolution and Bonding Properties of Electroplated Au/Sn/Au," Proceedings of The 2nd Electronics System-Integration Technology Conference (ESTC), 2008.
[12] K. Aasmundtveit, K. Wang, N. Hoivik, J. G. Graff and A. Elfving, “Au-Sn SLID Bonding: Fluxless Bonding with High Temperature Stability, to Above 350 ^{o}C”, Proceedings of IEEE-EMPC 2009, Rimini, Italy – June 14-17, 2009.
[13] J. Kim and C. Lee, “Fluxless Sn-Ag bonding in vacuum using electroplated layers”, Matererial Science and Engineering, Vol. A 448, pp 345-350, 2007.
[14] J. Kim, P. Wang and C. Lee, “Fluxless Bonding of Si Chips to Ag-Copper using Electroplated Indium and Silver Structures”, Proc. IEEE Advanced Packaging and Materials Symposium, pp 194-199, 2007.
[15] H. Liu, E. M. Husa, Z. Ramic, A. Munding, K. Aasmundtveit and N. Hoivik, “Uniformity requirements for electroplated Cu-Sn interconnects used in heterogeneous 3-D MEMS/ASIC stacks", in Proceedings of IMAPS Nordic, IMAPS, 2008.

IV